

<i>IMPORTANT</i> <i>DEFINITIONS</i>	<ul> <li>This is the safety alert symbol. It is used to alert you to potential personal injury hazards. Obey all safety messages that follow this symbol to avoid possible injury or death.</li> <li>DANGER—Indicates a hazardous situation which, if not avoided, will result in death or serious injury.</li> <li>WARNING—Indicates a hazardous situation which, if not avoided, could result in death or serious injury.</li> <li>CAUTION—Indicates a hazardous situation which, if not avoided, could result in minor or moderate injury.</li> <li>NOTICE—Indicates a hazard that could result in property damage only (including damage to the control).</li> <li>IMPORTANT—Designates an operating tip or maintenance suggestion.</li> </ul>	
<b>WARNING</b>	The engine, turbine, or other type of prime mover should be equipped with an overspeed shutdown device to protect against runaway or damage to the prime mover with possible personal injury, loss of life, or property damage. The overspeed shutdown device must be totally independent of the prime mover control system. An overtemperature or overpressure shutdown device may also be needed for safety, as appropriate.	
Read this entir installing, oper precautions. Fa	e manual and all other publications pertaining to the work to be performed before rating, or servicing this equipment. Practice all plant and safety instructions and ailure to follow instructions can cause personal injury and/or property damage.	
This publication you have the la The revision le version of mos If your publicat latest copy.	n may have been revised or updated since this copy was produced. To verify that atest revision, be sure to check the Woodward website: <u>www.woodward.com/pubs/current.pdf</u> vel is shown at the bottom of the front cover after the publication number. The latest at publications is available at: <u>www.woodward.com/publications</u> tion is not there, please contact your customer service representative to get the	
Any unauthorized modifications to or use of this equipment outside its specified mechanical, electrical, or other operating limits may cause personal injury and/or property damage, including damage to the equipment. Any such unauthorized modifications: (i) constitute "misuse" and/or "negligence" within the meaning of the product warranty thereby excluding warranty coverage for any resulting damage, and (ii) invalidate product certifications or listings.		
NOTICE	To prevent damage to a control system that uses an alternator or battery-charging device, make sure the charging device is turned off before disconnecting the battery from the system.	
NOTICE	To prevent damage to electronic components caused by improper handling, read and observe the precautions in Woodward manual 82715, <i>Guide for Handling and</i> <i>Protection of Electronic Controls, Printed Circuit Boards, and Modules</i> .	

Revisions—Text changes are indicated by a black line alongside the text.

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## **Distributed I/O**

The AtlasPC<sup>™</sup> control supports industry standard field bus protocols to take advantage of distributed I/O products from alternate manufacturers. Through various networking options, expansion of the AtlasPC system is virtually unlimited. Currently, the AtlasPC control supports:

- PC104 Profibus Interface (Chapter 1)
- PC104 DeviceNet Interface (Chapter 2)
- PC104 Ethernet Interface (Chapter 3)
- Serial (Modbus) Interface (Chapter 4)
- PC104 CanOpen Interface (Chapter 5)



Chapter 6 contains examples of Distributed I/O.

## Chapter 1. PC104 Profibus Interface

### Introduction

This chapter has been divided into two sections, Hardware for End Users, and Software for Application Developers. The hardware section is aimed at customers that are applying the Atlas in a permanent installation. The software section is for customers that are developing software for the AtlasPC<sup>™</sup> control.

### **Profibus Software and Hardware Requirements**

- Atlas with Profibus Module
- Profibus Master Configuration Tool
- Profibus Diagnostic Utilities
- Profibus slave device GSD file(s)
- GAP Programming Tool 3.03 or later
- Profibus Cables and Connectors
- Slave Interface and Modules
- Device Memory Maps and Scaling (Manuals)
- Woodward Interface Tools

### Hardware for End Users

### **Profibus Module**

The Profibus hardware module used on the AtlasPC control system is a PC/104 form factor ApplicomIO PC104-DPIO board, equipped with one Profibus port, capable of handling Profibus-DP (Distributed Peripherals) protocol in both Master (Class1, Class2) and Slave modes up to 12Mbps. This module operates on the PC104 bus and has a PC104 pass through connector to allow use with other PC104 modules depending on the Atlas configuration.

### **Electrical and Technical Specifications**

Processor:	Intel 80386EX, 24 MHz
Memory:	4 Mbyte DRAM, 512 K flash memory
Network Speeds Supported:	9600 kbps to 12 Mbps
Interface:	RS-485 with 500 Vdc galvanic isolation
Interface Connector:	Isolated DB9F I/O connector
Power:	4.0 W max (3.75 W typical)

### Interface Cables and Connectors

The Profibus network is a balanced transmission line corresponding to the standard EIA RS-485, terminated at both ends. The Profibus standard EN50170 defines two variations of the bus cable for Profibus-FMS and Profibus-DP. Profibus Type A cable is preferred and recommended for all uses.

- **Type A**—recommended for high transmission speeds (> 500 kBaud) and permits doubling of the network distance in comparison to Type B.
- **Type B**—should only be used at low baud rates and low requirements on the network distances.

Impedance:	135 up to 165 $\Omega$ at a frequency of 3 to 20 MHz	
Cable capacitance:	< 30 pF/m	
Core diameter:	> 0.34 mm <sup>2</sup> , corresponds to 22 AWG	
Cable type:	twisted pair cable. 1x2 or 2x2 or 1x4 lines	
Resistance:	< 110 Ω/km	
Signal attenuation:	: max. 9 dB over total length of line section	
Shielding:	CU shielding braid or shielding braid and foil	

Table 1-1.	Profibus-	–Туре А	Cable
------------	-----------	---------	-------

Impedance:	135 up to 165 $\Omega$ at a frequency of > 100 kHz
Cable capacitance:	typ. < 60 pF/m
Core diameter:	> 0.22 mm <sup>2</sup> , corresponds to 24 AWG
Cable type:	twisted pair cable. 1x2 or 2x2 or 1x4 lines
Signal attenuation: max. 9 dB over total length of line section	
Shielding:	CU shielding braid or shielding braid and foil

Table 1-2. Profibus—Type B Cable

#### **Recommended Bulk Cable**

Cable manufacturer Belden is widely available in North America, and Siemens is available in Europe. These manufacturers are listed in the table below. Neither manufacturer has any exclusive rights to Profibus cable, and other suitable alternatives are available from other manufacturers. Both cables below are rated as suitable for Profibus cabling and may also be used for drop cabling. Alternative cables may not use the same color coding on the individual conductors.

Manufacturer	Part Number	Website
Belden	3079A Profibus Cable	www.belden.com
Siemens	Profibus-DP, STD, 6XV1830- 0EH10	www.ad.siemens.de/simatic

The cable specification below is provided for convenience and is typical for the Profibus industry.

Belden 3079A Profibus Cable	
Weight:	57 lbs/1,000 ft (~85 kg/1000 m)
Ratings:	NEC PLTC CL2 CMG CEC CMG
Conductor:	#22 AWG solid high conductivity Cu (~0.3 mm <sup>2</sup> )
Insulation:	Cellular Polyethylene
Tested:	300 MHz
Nom. O.D.:	0.315" (8.00 mm)
Shield:	Beldfoil®, 100% coverage
Jacket:	Purple or Gray, PVC, optional blue intrinsically safe
Impedance:	150 Ω
Velocity Of Prop. :	78% (nom.)
Mutual Capacitance:	9.0pF/ft (nom.) (~30 pF/m)
Attenuation:	0.27 dB/100 ft @ 0.2 MHz (~0.89 dB/100 m)
	0.67 dB/100 ft @ 4.0 MHz (~2.20 dB/100 m)
	1.37 dB/100 ft @ 16.0 MHz (~4.49 dB/100 m)
	3.75 dB/100 ft @ 100 MHz (~12.30 dB/100 m)
	6.52 dB/100 ft @ 300 MHz (~21.39 dB/100 m)
Standard Lengths:	1000, 2000, and 3600 ft (~305, 610, and 1097 m)

Table 1-3. Belden Profibus cable

### **Profibus Cable Connectors**

The typical Profibus cable connector is a sub-D 9-pin male connector. The following products are provided for reference.

### Recommended Connector

Manufacturer	Part Number	Website	
Siemens	Bus Connector 6ES7 972-0BA11-0XA0	www.ad.siemens.de/simatic	
Olemens		www.au.sicmens.ue/simatic	

#### **Alternate Connectors**

Manufacturer	Part Number	Website
ERNI	Erbic PROFIBUS Connectors	www.erni.com
Siemens	Bus Connector 6GK1500-0EA02	www.ad.siemens.de/simatic
Phoenix Contact	SUBCON Profibus Connector–2744348	www.phoenixcon.com

#### **Profibus Connector Specifications**

The following connectors are typical for Profibus and are provided for reference.

Name:	Bus Connector	www.ad.siemens.de/simatic
Mfr:	Siemens	
P/N:	6ES7 972-0BA11-0XA0	A CONTRACT OF A
Connector:	DB9M	Contraction of the second second
Transmission Rate:	12 Mbits/sec	Harrison and the second second
Shielding:	Plastic case with internal shld clamp	the second second second second
Bus Termination:	Terminating resistor slide switch	
Cable Ports:	(2) for daisy chain use, 90° exit	
Cable Connection:	4 Internal screw terminal blocks	
Dim (WxHxD):	15.8 mm x 54 mm x 34 mm	11111

Table 1-4. Profibus—Siemens RS-485 Bus Connector / Plastic

Name:	Bus Connector	www.ad.siemens.de/simatic
Mfr:	Siemens	
P/N:	6GK1500-0EA02	
Connector:	DB9M	
Transmission Rate:	12 Mbits/sec	
Shielding:	Metal case with internal shld clamp	1 3
Bus Termination:	Terminating resistor slide switch	
Cable Ports:	(2) for daisy chain use	
Cable Connection:	4 Internal screw terminal blocks	
Dim (WxHxD):	15 mm x 57 mm x 39 mm	

Table 1-5. Profibus—Siemens RS-485 Bus Connector / Metal

### **Profibus Connector Pinout**

Connector	Signal Mnemonic
DB9F	Shielded DB9 female receptacle
1	
2	
3	RxD/TxD—P
4	
5	GND
6	+5 V
7	
8	RxD/TxD—N
9	
Shield	AC coupled to Earth Ground

Table 1-6. I/O Connector Pinout

### **Profibus Slave Hardware**

The AtlasPC control system can control Profibus slave modules from many different manufacturers. With the exception of Woodward-manufactured devices, Woodward makes no expressed or implied statement of suitability of these devices. It is the user's responsibility to ensure EMC compliance of their system, if necessary, by using distributed modules that are CE compliant. The following Profibus slave hardware has been tested with the AtlasPC control to confirm functionality.

1) All Woodward devices designed for Profibus

### AtlasPC Digital Control, Vol. II (Distributed I/O)

2) Allen-Bradley Fl			
	the second se		
Part Number	Description		
Part Number 3170-PDP	Description I/O Network Interface for Profibus (Slave) (ProSoft Technologies)		
Part Number           3170-PDP           1794-IB16	Description I/O Network Interface for Profibus (Slave) (ProSoft Technologies) Discrete Input (Sink)		
Part Number           3170-PDP           1794-IB16           1794-OV16	Description           I/O Network Interface for Profibus (Slave) (ProSoft Technologies)           Discrete Input (Sink)           Discrete Output (Sink)		
Part Number           3170-PDP           1794-IB16           1794-OV16           1794-OW8	Description         I/O Network Interface for Profibus (Slave) (ProSoft Technologies)         Discrete Input (Sink)         Discrete Output (Sink)         Discrete Output (Relay)		
Part Number           3170-PDP           1794-IB16           1794-OV16           1794-OW8           1794-IE8/B	Description         I/O Network Interface for Profibus (Slave) (ProSoft Technologies)         Discrete Input (Sink)         Discrete Output (Sink)         Discrete Output (Relay)         Analog Input (Current)		
Part Number           3170-PDP           1794-IB16           1794-OV16           1794-OW8           1794-IE8/B           1794-OE4/B	Description         I/O Network Interface for Profibus (Slave) (ProSoft Technologies)         Discrete Input (Sink)         Discrete Output (Sink)         Discrete Output (Relay)         Analog Input (Current)         Analog Output (Current)		
Part Number           3170-PDP           1794-IB16           1794-OV16           1794-OW8           1794-IE8/B           1794-OE4/B           1794-IT8	Description         I/O Network Interface for Profibus (Slave) (ProSoft Technologies)         Discrete Input (Sink)         Discrete Output (Sink)         Discrete Output (Relay)         Analog Input (Current)         Analog Output (Current)         Thermocouple Input		
Part Number           3170-PDP           1794-IB16           1794-OV16           1794-OW8           1794-IE8/B           1794-OE4/B           1794-IT8           1794-CJC2	Description         I/O Network Interface for Profibus (Slave) (ProSoft Technologies)         Discrete Input (Sink)         Discrete Output (Sink)         Discrete Output (Relay)         Analog Input (Current)         Analog Output (Current)         Thermocouple Input         Cold Junction		
Part Number           3170-PDP           1794-IB16           1794-OV16           1794-OW8           1794-IE8/B           1794-OE4/B           1794-IT8           1794-CJC2           1794-IR8	Description         I/O Network Interface for Profibus (Slave) (ProSoft Technologies)         Discrete Input (Sink)         Discrete Output (Sink)         Discrete Output (Relay)         Analog Input (Current)         Analog Output (Current)         Thermocouple Input         Cold Junction         RTD Input		
Part Number           3170-PDP           1794-IB16           1794-OV16           1794-OW8           1794-IE8/B           1794-OE4/B           1794-JT8           1794-IT8           1794-JCJC2           1794-IR8           1794-IB3S	Description         I/O Network Interface for Profibus (Slave) (ProSoft Technologies)         Discrete Input (Sink)         Discrete Output (Sink)         Discrete Output (Relay)         Analog Input (Current)         Analog Output (Current)         Thermocouple Input         Cold Junction         RTD Input         Terminal Base		

### 3) Automation Direct Terminator I/O

Part Number	Description
T1K-01AC	Power Supply
T1K-01DC	Power Supply
T1H-PBC	Profibus Interface
T1K-08ND3	Discrete Input (Sink)
T1K-16ND3	Discrete Input (Sink)
T1K-16TD1	Discrete Output
T1K-08TRS	Discrete Output (Relay)
T1F-16AD-1	Analog Input (Current)
T1F-16DA-1	Analog Output (Current)

Thermocouple Input Terminal Base

Terminal Base

T1F-14THM T1K-08B-1

T1K-16B-1

### **Software for Application Developers**

**WARNING** It is possible to disrupt an existing Profibus network by attaching an improperly configured device. To prevent problems on your existing Profibus network, read this chapter before connecting the AtlasPC Profibus port to a network.

IMPORTANT	Many end users will be purchasing pre-programmed AtlasPC units and will not need the information in this section. The information below is aimed at programmers using the GAP programming tool provided by Woodward. The information provided here covers the basics. For more detail, refer to Woodward software manual 26103, <i>Woodward NT Real Time Operating System Service and Interface</i> <i>Tools</i> or software manual 26199, <i>Woodward VxWorks Real Time</i>
	Operating System.

The information in this section is intended for customers that create their own GAP programs for the AtlasPC platform and who are using a Profibus network.

Programmers will need the following:

- ApplicomIO configuration software CD-ROM (supplied with the AtlasPC control)
- GSD file(s) for slave module(s)
- Device memory maps and scaling (manuals)
- GAP<sup>™</sup> Programming Tool 3.03 or later to create the application (This can be downloaded from our website: **www.woodward.com/ic/software**)
- For more information on these and additional software tools mentioned in this chapter, see Woodward software manual 26103 (NT RTOS) or 26199 (VxWorks RTOS).

The AtlasPC control is configured to communicate with a Profibus network by performing the following steps:

- 1. Verify that the Atlas contains a Profibus module.
- 2. Determine slave and I/O modules to be used.
- 3. Determine order of I/O modules.
- 4. Obtain GSD file(s).
- 5. Create Profibus Configuration using the Profibus Configuration Tool.

6. Review the Profibus slave manuals and understand the hardware addressing.

- 7. Create GAP application which reads and writes to the Profibus I/O.
- 8. Transfer Configuration files and GAP application to AtlasPC control.
- 9. Start GAP application.

#### Profibus Software Configuration (Configuration)

The Profibus network is configured using a Profibus Configuration Tool provided on CD-ROM with the AtlasPC control (ApplicomIO 2.1 Console). This tool supports defining the AtlasPC Profibus board as a master or slave device. For master operation, the slave devices are defined and configured by importing their GSD files and assigning network addresses. Once the Profibus I/O configuration is completed, it must be downloaded to the AtlasPC control and stored with the GAP application. The Profibus master interface card in the AtlasPC control is manufactured by Applicom International. All Applicom cards used in AtlasPC systems share IRQ 5. Even though they can use other IRQ settings, it is necessary that they share IRQ 5 for proper operation and to prevent conflict with other devices in the AtlasPC system. All IRQs are factory set and must not be changed by the end user.

All Applicom cards used in AtlasPC systems must use the same Base Address of D4000 when configured in the ApplicomIO Console software. The following example will show how to use the Applicom configuration tool.

- a. Run ApplicomIO 2.1 Console.
- b. Under File, select Configuration Manager. Select New if a new configuration is desired, or select an existing configuration listed. In this example, the configuration was named Config01. Application will close and require a restart when a new configuration is selected.

applicomIO⊕ console				
File Description ?				
Description (CONFIG01)      Boards configuration      DDE server parameters      OPC server parameters				
© ≫ № € Not available.				
Equipment Library 🙀 Network Detection				
Output Message View				
Ready	Configured boards state :	1		MAJ NUM DEF

- c. Under Board Configuration, select Add Board.
- d. Under Add New Board, select Diagnostic and Manual Configuration.

Add New Board	? ×
Board 1 Board to Add Board Type : ABSENT PC104/ISA Board Parameters DPRAM Base Address : D4000 Y Interrupt Vector : NONE Y Diagnostic and Manual Configuration »	Informations No board 1 was detected. Press the "Diagnostic and Manual Configuration" button to have more information or to manually configure this one.
	OK Cancel Help

e. Select DPRAM Base Address D4000, Interrupt Vector IRQ 5, and PC104/ISA PC104\_DPIO.

Add New Board	? ×
Board 1	
Board to Add Board Type : PC104_DPI0 PC104/ISA Board Parameters DPRAM Base Address : D4000 ▼ Interrupt Vector : IRQ 5 ▼ Diagnostic and Manual Configuration «	Informations No board 1 was detected. Press the "Diagnostic and Manual Configuration" button to have more information or to manually configure this one.
Detected Board(s) Board Name Properties Others	Manual Configuration C CompactPCI /PCI PC104_DPI0 PC104_CANIO PC104_DVNIO PC104/ISA
	OK Cancel Help

f. Select OK.

applicomIO® console			
File Description Library Network Protocol Items ?			
	JS Master - Station: 000 - 9.6 kbit/s		
	ej Local DP Slave		
므 🤫 Description (CONFIG01)			
E Boards configuration			
Protocol : PROFIBUS DP			
DDE server parameters			
PC server parameters			
Contraction			
ABB-DRIVES			
Applicom international			
DANFOSS DRIVES A/S			
Endress + Hauser			
Endress + Hauser Conducta			
Contrast Hauser Flowtec Ali      EUROTHERM			
EUROTHERM Automation			
Equipment Library 🙀 Network Detection			
WARNING : No configuration files found	WARNING : No configuration files found		
Looung congulation mes complete			
utput Message View			
Ready	Configured boards state : 1 MAJ NUM DEF		

#### AtlasPC Digital Control, Vol. II (Distributed I/O)

- g. Under Protocol, select Properties.
- h. Select 12 Mbit in Baud Rate.

Profibus Mast	er	? ×
General Confi	guration Advanced Configura	ation
Baud Rate :		12 Mbit/s
Master Profi	bus Address (0-126) :	000 💌
Highest Stat	ion Address (HSA:2-126) :	126 💌
Number of F	Repeaters (0-3) :	0 🔽
	Help	OK Cancel

i. Select OK.

Before a slave head (Network Interface Module) can be selected, the associated GSD file must be in the equipment library. If the GSD file doesn't already exist in the library, it must be downloaded and saved within the Applicom setup files (C:\Program Files\ApplicomIO\2.1\Equipment Library\Profibus\_gsd). In this example, the ProSoft 3170-PDP GSD file (psft0882.gsd) is imported using library, Add.

j. Select the 3170-PDP head under ProSoft Technology Inc. and drag to the window on the right. This will open a 3170-PDP setup window.

d applicom/U® console	
File Description Library Network Protocol Items ?	
	田一貫 [001] Station: 001 3170-PDP     □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □
E P Description (CONFIG01)	
Boards configuration	
Protocol : PROFIBUS DP	
DDE server parameters	
EUROTHERM Process Automation	
FESTO AG&Co.      F     GE Fanue	
GE Fanuc Automation NA, Inc.	
Horner Electric     Master Grabble	
E Murrelektronik	
OMRON Corporation	
3170-PDP	
Equipment Library 🕺 Network Detection	
Compared a country for restance account	
Loading configuration files	
Loading configuration files complete	
	<u>▼</u>
Dutput Message View	
Ready	Configured boards state : 1 MAJ NUM DEF

[000] - 3170-PDP			? ×
General Configuration GSD Informati	on Parameters Modules Co	onfiguration	
Identification			
Equipment: 001	🔽 Link	✓ Active	
Station : 001			
Parameters			
Watchdog Control (0-255) :	50 x 100 ms		
Data Format :	Big Endian (Motorola) 💌		
Description			
		<u></u>	
<u></u>			
	Help	OK Can	cel

- k. In this example the Station number is selected as 001. (This is what is referred to as the node number.)
- I. Select the Modules Configuration Tab.

[000] - 3170-PDP				?	×
General Configuration GSD Infor	mation   F	arameters	Modules Config	guration	
- Informations					
Input Size (0-244) :	Byl	es Mo	dule Count (1-9)	: 0	
Output Size (0-244) :	Byl	es			
Data Size (1-488) : 0	Byl	es			
Available Module(s)	Input	Output C	Configuration		
Flex I/O empty slot	0	0 0	0 00		
8 3170-PDP 1.2 Status	2	2 5	0 60	Add	11
8 1794-IA8	2	2 5	0 60		1
🔆 1794-IA8I	2	2 5	0 60	_1	
	•	о г	* 00		
Configured Module(s) Input	Output C	onfiguration	า	Remove	ıL
					4
				Move Up	
				Maria Draum	ıL.
				Move Down	Ч
		Help	OK	Cancel	
					_

m. Build the module configuration by dragging the desired modules from the Available Module(s) window to the Configured Module(s) window.

00] - 3170-PDP					?
General Configuration   GSD In	nformation	Parameter	s Module	s Configuratio	n
Informations					
Input Size (0-244) :	68 E	Bytes M	lodule Cou	nt (1-9) :	8
Output Size (0-244) :	38 E	Bytes			
Data Size (1-488) :	106 E	Bytes			
Available Module(s)	Inpu	t Output	Configura	tion 🔺	
🔆 1793-0W4(S)	0	2	00 60		
8 1794-IR8	22	6	5A 62		bbA
🔆 1794-IRT8	22	8	5A 63		
😵 1794-IT8	22	8	5A 63		
		40	FC 07	<u></u>	
Configured Module(s) In	put Outpu	ıt Configu	ration	▲	Bemove
😵 3170-PDP 1.2 Status - 2	2	50 60			
😵 1794-IB16 2	2	50 60			Move Up
9 1794-0∨16 0	4	00 61			-
😵 1794-0W8 0	2	00 60		-	Move Dow
10A 47040E0 44	· ^	F0.00		<u>·</u>	
		Help		ок	Cancel

n. Select OK when done.

applicomIO@ console	
File Description Library Network Protocol Items ?	
Pescription (CONFIG01)     Baards configuration     Pescription (CONFIG01)     Pescription (CONFI	Image: Property of the state of th
Figurinment Library Rel Network Detection	
Adding file(s) Adding file(s) complete	۸ ۲
Dutput Message View	
Ready	Configured boards state : 1 MAJ NUM DEF

o. This completes the Applicom setup.



Once created, the Profibus configuration files can be found on the programming station under c:\program files\applicomIO\2.1\configIO\config\_name.

🔁 Config01			_ 🗆 🗵				
File Edit View Favorites Tools	File Edit View Favorites Tools Help						
📙 🖙 Back 👻 🤿 👻 🔂 🔯 Search	🔁 Folders 🛛 🛞 History 🛛 😤 😤 🗙	vn <b>≣</b> •					
Address 🗀 C:\Program Files\applicomIC	1\2.1\configI0\Config01		💌 🤗 Go				
Adminmsg.041	Adminmsg.042	🚮 Adminmsg.04	3				
Adminmsg.044	Adminmsg.045	🖬 Adminmsg.04	6				
Adminmsg.047	Adminmsg.048	폙 apDbParam.z	z				
ApDbParam1_0.Bin	ApDbParam1_0.Def	APPLICOM.INI					
🐻 appusr.ini	T CNFDP01.101	CNFMAST.001					
🝙 confapli.ap1	🖬 confapli.ap2	🝙 confapli.ap3					
👼 confapli.ap4	🖬 confapli.ap5	👼 confapli.ap6					
🔊 confapli.ap7	a] confapli.ap8	configuration	board1 channel0.lst				
🖬 ConfTag1_0.Bin	🔚 ConfTag1_0.Def	📓 DescCnf.ini					
general configuration.lst	item configuration board1 channel0.lst	🛒 motorio.ini					
30 object(s)		224 KB	🖳 My Computer //				

p. Save the configuration and copy all files from the ConfigIO directory to the AtlasPC control using AppManager. (C:/Woodward/Applications directory)

#### Profibus Software Configuration (GAP)

After creating the Profibus I/O configuration, the GAP application must be programmed to match. The steps necessary to program the Profibus module in GAP are as follows:

a. Select FB\_MODULE for slot 6 in the GAP application. All FieldBus modules use the same Parent Block.

ATLA	<b>s</b> -	"_M	AST	ER.0	:н"								×
C <u>a</u> te <u>o</u> Block	gory: : <u>N</u> an	ne:	[ 	_MA: CH	STER	3		<u>K</u> ern Cha <u>s</u> s	el:   is:  1	<u>E</u> dit Na <u>D</u> elei	ame te	<u> </u>	<u>)K</u> ncel
Bjock	:			Þ	·					<u>B</u> rano	sh	H	elp
A1	A2	AЗ	Α4	A5	A6	A7							
CPU					FBM								
NTICPU					FB MODULE								

b. Select a FB\_EQUIP Block for every node in the Network and list it in the FB\_MODULE Parent Block. Every FB\_EQUIP block must have its EQUIP\_NO set to the Station number of its respective node.

For examples of a complete GAP setups for Profibus, see the Distributed I/O Examples later in this chapter.

- c. Once completed, the GAP application must be compiled and downloaded to the AtlasPC control using AppManager.
- d. Once the GAP application is started on the AtlasPC control's PC, the Profibus module will automatically initialize and start the Profibus Network. All nodes will be updated from the Applicom module in a circular queue fashion, once every scan rate. The GAP application will update its values once every rate group (defined in FB\_MODULE).



The timing of the Applicom scan rate will depend on the number of groups (heads) and the number of nodes (I/O modules) in the network and will be independent of the rate group structure.

## Chapter 2. PC104 DeviceNet Interface

### Introduction

DeviceNet and CanOpen are protocols that uses CAN (Controller Area Network). This chapter describes the DeviceNet protocol only and has been divided into two sections, Hardware for End Users, and Software for Application Developers. The hardware section is aimed at customers that are applying the Atlas in a permanent installation. The software section is for customers that are developing software for the AtlasPC<sup>™</sup> control.

### **DeviceNet Software and Hardware Requirements**

- Atlas with DeviceNet Module
- DeviceNet Master Configuration Tool
- DeviceNet Diagnostic Utilities
- DeviceNet slave device EDS file(s)
- GAP Programming Tool 3.03 or later
- DeviceNet Cables and Connectors
- Slave Interface and Modules
- Device Memory Maps and Scaling (Manuals)
- Woodward Interface Tools

### Hardware for End Users

### **DeviceNet Module**

The DeviceNet hardware module used on the AtlasPC control system is a PC/104 form factor ApplicomIO PC104-DVNIO board, equipped with one DeviceNet port capable of handling DeviceNet protocol in both Master/Scanner and Slave modes up to 500 Kbps. This module operates on the PC104 bus and has a PC104 pass-through connector to allow use with other PC104 modules depending on the Atlas configuration.

### **Electrical and Technical Specifications**

Processor:	AMD SC520–100 MHz
Memory:	8 Mbytes dynamic RAM
Flash Memory:	512 Kbytes flash memory
Power:	5 W (max. 0.8A)

### **Interface Cables and Connectors**

Most users will purchase finished cables, but the following information is provided for users who need to build custom cables.

### AtlasPC Digital Control, Vol. II (Distributed I/O)

The ODVA standard for DeviceNet defines two variations of the bus cable that are compatible with the Phoenix COMBICON connector on the AtlasPC control— Thick and Thin types. The Thick cable is preferred and recommended for all uses. Most DeviceNet cable is not rated for temperatures above 80 °C, so be careful during installation to avoid hot routing areas. Always use the appropriate CAN cable for DeviceNet wiring. Alternate cables will very likely inhibit reliable communication.

- **Thick**—recommended for high transmission speeds and long network distance in comparison to Thin cable.
- **Thin**—should only be used at low baud rates and low requirements on network length. Thin cable should never be used on an engine in a vibration environment.

Impedance:	120Ω ±10% at 1MHz
Cable capacitance:	12 pF/ft at 1kHz
Propagation delay	1.36 ns/ft (maximum)
Data Pair:	19 strands, 1.0 mm <sup>2</sup> corresponds to 18 AWG, individually tinned, 3 twists/foot
Power Pair:	19 strands, 1.5 mm <sup>2</sup> corresponds to 15 AWG, individually tinned, 3 twists/foot
Drain / Shield Wire:	19 strands Tinned Copper shielding braid or shielding braid and foil
Cable type:	twisted pair cable. 2x2 lines
Bend Radius:	20 x diameter during installation or 7 x diameter fixed position
Signal attenuation:	0.13 dB/100 ft @ 125 kHz (maximum)
	0.25 dB/100 ft @ 500 kHz (maximum)
	0.40 dB/100 ft @ 1000 kHz (maximum)

Table 2-1. Thick Cable Requirements

### **Recommended Bulk Cable**

Cable manufacturer Belden is widely available in North America, and Lapp Cable products (Germany) is available in Europe, so these manufacturers are listed in the table below. Neither manufacturer has any exclusive rights to CAN cable, and other suitable alternatives are available from other manufacturers. All three cables below are rated as suitable for DeviceNet trunk cabling and may also be used for drop cabling. Alternative cables may not use the same color coding on the individual conductors.

Manufacturer	part number	Website
Belden	3082A DeviceNet Thick Cable–Grey	www.belden.com
Belden	3083A DeviceNet Thick Cable–Yellow	www.belden.com
Lapp Cable	2710-250 Unitronic DeviceNet Thick	www.lappcable.com

The cable specification below is provided for convenience and is typical for the DeviceNet industry.

Belden 3082A DeviceNet	
Cable	
Weight:	108 lbs/1,000 ft
Ratings:	UL PLTC, CMG, AWM, C(UL) AWM I/II A. Flame
_	Resistance: UL 1581, CSA FT4
Conductor:	#15/18 AWG Stranded (19x28)/(19x30)
Insulation:	PVC/Nylon/Foam PE–Polyvinyl
	Chloride/Nylon/Foam Polyethylene
Nom. O.D.:	0.46" (11.7 mm)
Shield:	Individual Aluminum Foil-Polyester Tape/Braid
Jacket:	Lt Gray, PVC
Impedance:	120 Ω
Velocity Of Prop. :	75% (nom.)
Mutual Capacitance:	12.0pF/ft (nom.) (~39 pF/m)
Attenuation:	.13 DB/100' @ 125 KHZ
	.25 DB/100' @ 500 KHZ
	.36 DB/100' @ 1 MHZ
Standard Lengths:	500, 1000, and 2000 ft

Table 2-2. Belden DeviceNet cable

#### **Cable Connectors**

The typical DeviceNet cable connector is a 5-pin open-style connector. The following products are provided for reference and are compatible with the AtlasPC interface connector.

Manufacturer	P/N	Website
Phoenix Contact	COMBICON MSTB 2.5/5-STF-5.08	www.phoenixcon.com

### **Connector Specifications**

General characteristics of connectors used for DeviceNet data cabling:

Plating:	762 nm (30 micro inch) gold minimum over 1270 nm (50 micro inch) nickel minimum or 127 nm (5 micro inch) gold minimum over 508 nm (20 micro inch) palladium-nickel minimum over 1270 nm (50 micro inch) nickel. All gold must be 24 karat
Resistance:	< 1 mΩ

If the CAN wiring is routed through a terminal block, the terminal block should have the above characteristics. The drain/shield should be maintained through the terminal block as well.

#### **DeviceNet Connector Pinout**



In the connector photo, the pinout from left to right is shown in the table from top to bottom. Other connectors may be used on some products.

Position	Color	Name	Size	Notes
1	Black	V(-)	1.5 mm <sup>2</sup> (15 AWG)	Used so all devices have
				a common reference
2	Blue	CAN-Low	1.0 mm <sup>2</sup> (18 AWG)	Data
3	None	Shield / Drain	1.0 mm <sup>2</sup> (18 AWG)	AC-coupled to the chassis
				of the AtlasPC control
4	White	CAN-High	1.0 mm <sup>2</sup> (18 AWG)	Data
5	Red	V(+)	1.5 mm <sup>2</sup> (15 AWG)	11–25 Vdc input required

Always ground the V(–) at only one point in the system. This point should be the same as the DeviceNet power supply ground.

### **Network Wiring**

CAN networks are multi-drop networks arranged with two physical ends and up to 64 nodes connected between the ends. Many limitations work together to define the total end-to-end length of the network. This section will help define those.

### Network Length

Length of the CAN cabling is variable depending on many factors. Cable type is one factor that significantly affects maximum length. Woodward recommends only the "thick" cable type which is capable of the maximum length.

CAN allows for a single trunk with drops to each (or multiple) nodes. The number of drops is not limited nor is the number of nodes applied on a single drop. However, the length of wire in each drop is limited. The length of any single drop may be 0 to 6 meters where a zero length drop means the node is attached directly to the trunk. The total length of all drops together (cumulative drop length) is limited by the cable type and the baud rate in use.



Figure 2-1. Typical CAN Network Example

The example below shows three methods of connecting a CAN device on the network. The example also includes a couple of devices that do not use the power pair in the CAN cable. Most devices require the power pair but some do not. Reference the device literature for details and requirements.

The table below gives the maximum trunk and cumulative drop lengths for each supported baud rate. Using less in one column does NOT allow usage of more in another column. Each column is exclusive and represents an absolute maximum.

Baud Rate	Trunk Length	Cumulative Drop	Maximum Drop
125 kb	500 m (1640 ft)	156 m (512 ft)	6 m (20 ft)
250 kb	250 m (820 ft)	78 m (256 ft)	6 m (20 ft)
500 kb	100 m (328 ft)	39 m (128 ft)	6 m (20 ft)

### **Terminating Resistors**

A termination resistor must always be present at each end of the network for the devices to communicate properly. CAN requires a terminating resistor to be installed at each end of the trunk—not at the end of a drop. The resistor requirements are:

- 121 Ω
- 1% Metal Film
- 0.25 W

The resistor must be installed between pins 2 and 4 (the CAN-Low and CAN-High pins) of the DeviceNet connector.



### IMPORTANT

Terminating resistors should not be installed at the end of a drop line. They should be installed only at the two ends of the trunk line.

Since termination resistors cannot be placed at the end of a drop line, the AtlasPC control is not provided with built-in network termination resistors.

### Shielding

Shielded cable must be used between the AtlasPC control and any other devices. Unshielded cables and improperly shielded cables will very likely lead to communication problems and unreliable control operation.

The shield must always be AC-coupled (connected through a capacitor or RC network) at each connected device and connected directly to earth ground for proper operation. The AtlasPC control has been constructed so that the Shield/Drain connection is AC-coupled to chassis ground internal to the AtlasPC control through a parallel combination of a 0.01  $\mu$ F capacitor and 1 M $\Omega$  resistor as defined by the DeviceNet standard. The installer must provide for connection directly to earth, or the shield must be run to a properly grounded stud at a single point on the network.

### 24 Volt Power Supply

The DeviceNet network is different from many others in that a 24 Vdc power supply is distributed with the network. The AtlasPC system does not provide this supply, and all customers using DeviceNet will have to provide a separate and isolated supply to ensure proper network operation.

The governing authority for DeviceNet (ODVA) has specific requirements for the 24 Vdc network supply. Select a supply that meets these requirements. Certified supplies can be found on the ODVA web site (www.odva.org).

### **DeviceNet Slave Hardware**

The AtlasPC control system can control DeviceNet slave modules from many different manufacturers. With the exception of Woodward-manufactured devices, Woodward makes no expressed or implied statement of suitability of these devices. It is the user's responsibility to ensure EMC compliance of their system, if necessary, by using distributed modules that are CE compliant. The following DeviceNet slave hardware has been tested with the AtlasPC control to confirm functionality.

1) All Woodward devices designed for DeviceNet

2) Allen-Bradley Fle	ex I/O
Part Number	Description
1794-ADM	I/O Network Interface for DeviceNet (Slave)
1794-IB16	Discrete Input (Sink)
1794-OV16	Discrete Output (Sink)
1794-OW8	Discrete Output (Relay)
1794-IE8/B	Analog Input (Current)
1794-OE4/B	Analog Output (Current)
1794-IT8	Thermocouple Input
1794-CJC2	Cold Junction
1794-IR8	RTD Input
1794-TB3S	Terminal Base
1794-TB3TS	Terminal Base

### 3) Automation Direct Terminator I/O

Part Number	Description
T1K-01AC	Power Supply
T1K-01DC	Power Supply
T1K-DEVNETS	DeviceNet Interface
T1K-08ND3	Discrete Input (Sink)
T1K-16ND3	Discrete Input (Sink)
T1K-16TD1	Discrete Output
T1K-08TRS	Discrete Output (Relay)
T1F-16AD-1	Analog Input (Current)
T1F-16DA-1	Analog Output (Current)
T1F-14THM	Thermocouple Input
T1K-08B-1	Terminal Base
T1K-16B-1	Terminal Base

### **Software for Application Developers**

|--|

IMPORTANT	Many end users will be purchasing pre-programmed AtlasPC units and will not need the information in this section. The information below is aimed at programmers using the GAP programming tool provided by Woodward. The information provided here covers the basics. For more detail, refer to Woodward software manual 26103, <i>Woodward NT Real Time Operating System Service and Interface Tools</i> or software manual 26199, <i>Woodward VxWorks Real Time Operating System.</i>
-----------	--

Programmers will need the following:

- ApplicomIO configuration software CD-ROM (supplied with the AtlasPC control)
- EDS file(s) for slave module(s)
- Device memory maps and scaling (manuals)
- GAP<sup>™</sup> Programming Tool 3.03 or later to create the application (This can be downloaded from our website: **www.woodward.com/ic/software**)
- For more information on these and additional software tools mentioned in this chapter, see Woodward software manual 26103 (NT RTOS) or 26199 (VxWorks RTOS).

The AtlasPC control is configured to communicate with a DeviceNet network by performing the following steps:

- 1. Verify that the Atlas contains a DeviceNet module.
- 2. Determine slave and I/O modules to be used.
- 3. Determine order of I/O modules.
- 4. Obtain EDS file(s).
- 5. Create a DeviceNet Configuration using the DeviceNet Configuration Tool.
- 6. Review the DeviceNet slave manuals and understand the hardware addressing.
- 7. Create GAP application which reads and writes to the DeviceNet I/O.
- 8. Transfer Configuration files and GAP application to AtlasPC control.
- 9. Start GAP application.

### DeviceNet Software Configuration (ApplicomIO Console)

The DeviceNet network is configured using the DeviceNet Configuration Tool provided on CD-ROM with the AtlasPC control (ApplicomIO 2.1 Console). This tool supports defining the AtlasPC DeviceNet board as a master or slave device. For master operation, the slave devices are defined and configured by importing their EDS files and assigning network addresses. Once the DeviceNet I/O configuration is completed, it must be downloaded to the AtlasPC control and stored with the GAP application.

The DeviceNet master interface card in the AtlasPC control is manufactured by Applicom International. All Applicom cards used in AtlasPC systems share IRQ 5. Even though they can use other IRQ settings, it is necessary that they share IRQ 5 for proper operation and to prevent conflict with other devices in the AtlasPC system. All IRQs are factory set and must not be changed by the end user.

All Applicom cards used in AtlasPC systems must use the same Base Address of D4000 when configured in the ApplicomIO Console software. The following example will show how to use the Applicom configuration tool.

- a. Run ApplicomIO 2.1 Console.
- b. Under File, select Configuration Manager. Select New if a new configuration is desired, or select an existing configuration listed. In this example, the configuration was named Config01. Application will close and require a restart when a new configuration is selected.

applicomIO® console		×
Eile Description ?		
Description (TEST)		
Boards configuration		
OPC server parameters		
Equipment Library		
		-1
		1
		1
, Dutrut Message View		
		r'
Ready	Configured boards state :	11

### AtlasPC Digital Control, Vol. II (Distributed I/O)

- C.
- Under Board Configuration, select Add Board. Under Add New Board, select Diagnostic and Manual Configuration. d.

Add New Board	<u>?</u> ×
Board 1	
Board to Add Board Type : PC104_DVNIO PC104/ISA Board Parameters DPRAM Base Address : D4000 Interrupt Vector : IRQ 5 Diagnostic and Manual Configuration «	Informations No board 1 was detected. Press the "Diagnostic and Manual Configuration" button to have more information or to manually configure this one.
Detected Board(s) Board Name  Properties Others	Manual Configuration CompactPCI /PCI PC104_DPI0 PC104_CANIO PC104_DVNIO PC104/ISA
	OK <u>C</u> ancel Help

e. Select DPRAM Base Address D4000, Interrupt Vector IRQ 5, and PC104/ISA PC104\_DVNIO.

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applicomIO® console	
File Description Library Network Protocol Ite	ms <u>?</u>
	📃 🔄 🔊 DeviceNet Master : MAC ID: 00 - Baud Rate: 125 Kbits/s
	INONE] DeviceNet Local Slave
E- 📅 Description (TEST)	
Boards configuration	
Board 1 PC104_DVNIO	
Protocol : DeviceNet	
OPC server parameters	
1	
🖃 🔚 Equipment Available	
AC Drives	
🗄 🕀 🔂 Barcode Scanner	
🗄 🚽 🔂 Communications Adapter	
🗄 🕀 🔂 Contactor	
🕀 🖓 Dodge EZLINK	
🗄 🖓 🔄 General Purpose Discrete I/O	
Human-Machine Intercate	
Inductive Proximity Switch	
🔄 Equipment Library 🙀 Network Detection	
Loading configuration files complete	
🛄 Output Message View	
Ready	Configured boards state : 1

f. Under Files --> Properties, Make sure Expert Mode is Checked.

g. Under Protocols, select Properties.

DeviceNet Master	<u>? ×</u>
General Configuration 1/0 Summa	ry
Baud Rate :	00 Kbits/s
MAC ID :	00 💌
Interscan Delay (2 - 9000) : 2	<u>★</u> ms <u>D</u> efault Values
Foreground to Background Poll Ratio (1- 32000) :	
Expert Mode	
Expected Packet Rate [10 (10 - 32000):	D 💌 ms
<u>H</u> e	elp <u>O</u> K <u>C</u> ancel

- h. Select the correct Values for the Network. The DeviceNet Net Timeout will be 4 times the expected packet rate, and must be set with care.
- i. Drag and Drop all nodes in the Network from the Equipment Library to the DeviceNet Master.

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001] - SPC		<u>? ×</u>
General Configuration EDS Information Connection Configuration EDS	Viewer	
Identification   Equipment :   MAC ID :   Otra     Parameters     Data Format :     Little Endian (Intel)     Description	Check Identification          Vendor ID         Product Type         Product Code         Revision	
<u>H</u> elp	<u>0</u> K <u>C</u> ar	ncel

- j. Select a unique MACID for each node
- k. Select Little Endian vs Big Endian.
- I. If a node cannot be found in the Library, It can be added using Library→ Add.

Select configu	iration files	<u>?</u> ×
Look jn: 🔂	Equipment Library 🔽 🖛 🗈 📸 🎫	
CanOpen_	eds	
DeviceNet_	_eds	
Profibus_g	sd	
File <u>n</u> ame:	<u>0</u> pe	n
Files of <u>type</u> :	DeviceNet Electronic Data Sheet (*.EDS)	el
		//

m. Select the EDS file supplied by the Nodes Manufacturer.

AtlasPC Digital Control, Vol. II (Distributed I/O)

[None] - DeviceNet Local Slave	<u>? ×</u>
General Configuration Connection Configuration EDS Viewer	
_ Identification	
Equipment : None	
Parameters 003	
Data Format 005 Little Endian (Intel)	
007 Description 008 009 ▼	
<< Previous Next >> Help OK Ca	incel

n. The Atlas can also be configured as a DeviceNet Slave, by selecting DeviceNet Local Slave. First Select a MACID.

[None] - DeviceNet Local Slave		? ×
General Configuration Connection Configur	ation EDS Viewer	
	Change Of State / Cyclic	
Output Size (0 - 8) : 0 Bytes	C C.O.S. C Cyclic	
✓ Polling Output Size (0 - 255): 32 Bytes	Output Size (0 - 255) : 0 Bytes	
Input Size (0 - 255) : 16 Bytes	Input Size (0 - 255) : 0 Bytes	
<< Previous <u>N</u> ext>>	<u>H</u> elp <u>O</u> K <u>C</u> ar	icel

- o. Then enter the relevant number of bytes in the appropriate fields.
- p. Once all nodes have been entered, select File  $\rightarrow$  Save.

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applicomIO® console	
<u>File Description Library Network Protocol Items ?</u>	
	8
Image: Second	Image: Construction of the system           Image: Constres           Image: Cons
Saving configuration files Saving configuration files complete	
🛄 Output Message View	
Ready	Configured boards state : 1

Copy all files from the ConfigIO directory to the AtlasPC control's PC q. using AppManager.

Once created, the DeviceNet configuration files can be found on the



### **DeviceNet Software Configuration (GAP)**

After creating the DeviceNet I/O configuration, the GAP application must be programmed to match. The steps necessary to program the DeviceNet module in GAP are as follows:

a. Select FB\_MODULE for slot 6 and or 7 in the Atlas Chassis. All FieldBus modules use the same Parent Block.

ATLAS -	"_MAST	FER.CH"			×
C <u>a</u> tegory: Block <u>N</u> a	me: [	_MASTEF	<u>K</u> ernel: Cha <u>s</u> sis:	1 <u>E</u> dit Name	Cancel
Bjock				<u>B</u> ranch	<u>H</u> elp
A1 A2	A3 A4	A5 A6	A7		
C P U		F B M			
N T C P U		FB I∑ODJIW			

b. Select a FB\_EQUIP Block for every node in the Network and list it in the FB\_MODULE Parent Block. Every FB\_EQUIP block must have it's EQUIP\_NO set to the MACID of its respective node.
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c. Every Node is then defined using specific GAP blocks (SPC, VPC, SWIFT) or generic blocks (FB\_AI, FB\_AO, FB\_BI, FB\_BO).



For examples of a complete GAP setups for DeviceNet, see the Distributed I/O Examples later in this chapter.

- d. Once completed, the GAP application must be compiled and downloaded to the AtlasPC control using AppManager.
- e. Once the GAP application is started on the AtlasPC control's PC, the DeviceNet module will automatically initialize and start the DeviceNet Network. All nodes will be updated from the Applicom module in a circular queue fashion, once every scan rate. The GAP application will update its values once every rate group (defined in FB\_MODULE).



The timing of the Applicom scan rate will depend on the number of groups (heads) and the number of nodes (I/O modules) in the network and will be independent of the rate group structure.

### Chapter 3. PC104 Ethernet Interface

### Introduction

This chapter has been divided into two sections, Hardware for End Users, and Software for Application Developers. The hardware section is aimed at customers that are applying the Atlas in a permanent installation. The software section is for customers that are developing software for the AtlasPC<sup>™</sup> control.

The AtlasPC control has one Ethernet port on the CPU and one optional PC104 Ethernet board. If the second PC104 Ethernet board is installed, it can be used for either Modbus<sup>®</sup> \* communication with an HMI, distributed I/O, or redundant control. Redundant Ethernet is used with the GE EGD package for sequencing controls. Either Ethernet port may be used for distributed I/O, but it is recommended that only the PC104 Ethernet port be use for this purpose. The CPU Ethernet port is the only Ethernet port accessible with AppManager. Each port uses a different IP address that can be set by AppManager. This subchapter deals primarily with distributed I/O connections. For more information on HMI communications and redundant controls, consult appropriate vendor manuals.

\*—Modbus is a trademark of Schneider Automation Inc.

### **Ethernet Software and Hardware Requirements**

- Atlas with PC104 Ethernet Module
- GAP Programming Tool 3.03 or later
- Ethernet Cables and Connectors
- Slave Interface and Modules
- Device Memory Maps and Scaling (Manuals)
- Woodward Interface Tools

### Hardware for End Users

### **Ethernet Module**

To use with distributed I/O, the AtlasPC control may be configured as a Modbus master using Ethernet UDP or Ethernet TCP/IP. Grayhill distributed I/O, Modicon distributed I/O, and Bentley-Nevada vibration systems use Ethernet TCP/IP protocol and are compatible with the AtlasPC control. Currently, neither Allen-Bradley nor Automation Direct distributed I/O are able to interface with the AtlasPC control over Ethernet because they use an incompatible protocol.

The PC104 Ethernet port is an auto-switching 10/100 Megabit per second (Mbps) connection accessed through a second RJ45 connector labeled Ethernet #2. It complies with IEEE/ANSI 802.3 and Blue Book standards. If 100 Megabit operation is desired, all devices on the network must be 100 Base-TX capable.

The PC104 Ethernet module used in the AtlasPC control system is a PC/104 form factor module supporting TCP/IP and UDP protocols. This module operates on the PCI bus but it has both PCI and PC104 pass through connectors to allow use with other PCI and PC104 modules, depending on the Atlas configuration.

### **Electrical and Technical Specifications**

Controller:	AMD 79C973	
Memory:	12 Mbytes dynamic RAM	
Bus Interface:	32 bit PC/104 Plus bus	
Voltage:	5.0 Vdc only	
Power:	1.5 W Typical	

### **Interface Cables and Connectors**

Most users will purchase finished cables, but the following information is provided for users that need to build custom cables.

The AtlasPC control requires double-shielded cable (SSTP) for Ethernet in order to be appropriately immune to EMC in industrial environments. Below are the general requirements for Category 5 Ethernet cable.

Impedance:	100.0 Ω ±15%
Cable capacitance:	49.2 pF/m (15.0 pF/ft) at 1 kHz
Propagation Velocity:	67.0%
Data Pairs:	0.2 mm <sup>2</sup> (24 AWG) solid bare copper
Cable type:	Category 5 compatible with RJ45
Bend Radius:	25 mm (1.0 inch)
Signal attenuation:	2.0 dB/100 m at 1.0 MHz

Table 3-1. Category 5 Cable Requirements

#### **Recommended Bulk Cable**

Since cable manufacturer Belden is widely available, their cable types are listed as a reference. Belden has no exclusive rights to Ethernet cable, and other suitable alternatives are available from other manufacturers. Both cables below are rated as suitable for Ethernet category 5 cabling and compatible with RJ45 connectors.

Manufacturer	P/N	Website
Belden	1624P Ethernet DataTwist 5	www.belden.com
Belden	1624R Ethernet DataTwist 5	www.belden.com

The cable specification below is provided for convenience and is typical for the Ethernet industry.

Belden 1624P Ethernet		
Cable		
Weight:	34 lbs/1,000 ft	
Ratings:	UL/NEC TYPE CMP, CEC C(UL) CMP, TIA/EIA	
	568A CAT 5, UL VERIFIED TO CAT 5, NEMA WC-	
	63.1 CAT 5	
Conductor:	#24 AWG Solid	
Insulation:	FEP–Fluorinated Ethylene Propylene	
Nom. O.D.:	0.24" (6 mm)	
Shield:	Aluminum Foil-Polyester Tape	
Jacket:	FA–FLAMARREST(TM) PVC	
Impedance:	100 Ω	
Velocity Of Prop. :	67% (nom.)	
Mutual Capacitance:	15.0pF/ft (nom.) (~49 pF/m)	
Attenuation:	1.8 DB/100 Mtrs @ .772 MHz	
	2.0 DB/100 Mtrs @ 1.0 MHz	
	4.1 DB/100 Mtrs @ 4.0 MHz	
	5.8 DB/100 Mtrs @ 8.0 MHz	
	6.5 DB/100 Mtrs @ 10.0 MHz	
	8.2 DB/100 Mtrs @ 16.0 MHz	
	9.3 DB/100 Mtrs @ 20.0 MHz	
	10.4 DB/100 Mtrs @ 25.0 MHz	
	11.7 DB/100 Mtrs @ 31.25 MHz	
	17.0 DB/100 Mtrs @ 62.5 MHz	
	22.0 DB/100 Mtrs @ 100 MHz	
Standard Lengths:	1000 ft	

Table 3-2.	Belden	Ethernet	cable
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### **Cable Connectors**

The typical Ethernet cable connector is an RJ45 style connector. The following products are provided for reference and are compatible with the AtlasPC RJ45 interface connector.

Manufacturer	P/N	Website
Tyco Electronics (Amp)	5-569550	www.amp.com

#### Ethernet Connector Pinout

Connector	Signal Mnemonic
RJ45F	Shielded RJ45 female
	receptacle
1	TX+
2	TX-
3	RX+
4	
5	
6	RX-
7	
8	
Shield	AC Coupled to Chassis GND

Table 3-3. RJ45 10/100 Base-TX Pinout

NOTICE

Use shielded Ethernet cable only! Use of non-shielded cable may result in permanent system damage.

### **Network Wiring**

There are two possible connection setups for the Ethernet networks.

The first is a network consisting of an Atlas and one other device with no routers, switches, or other external devices. In this configuration the cable between Atlas and the other device must be a crossover cable. A crossover cable has the following pin connections:

Connector 1 Pin #	Connector 2 pin #
1	3
2	6
3	1
4	4
5	5
6	2
7	7
8	8



Crossover cables can often be spotted visually by comparing the connectors side by side. If a colored wire is found on one pin of the first connector, but on a different pin of the second connector, the cable is probably a crossover cable.

In the second type of network there will be at least two devices plus a router, hub, server, or switch. This type of network will use straight-through cables, meaning that pin 1 on one connector is connected to pin 1 on the other.

The 100BASE-TX media system is designed to allow segments of up to 100 meters in length when using data grade twisted-pair wire that has a characteristic impedance of 100 ohms and meets the EIA/TIA Category Five wire specifications. Segments of 100BASE-TX are limited to a maximum of 100 meters to ensure that the round-trip timing specifications are met. This is in contrast with the 10BASE-T media system, where the maximum segment length for the 10-Mbps link is mostly limited by signal strength. The EIA/TIA cabling standard recommends a segment length of 90 meters between the wire termination equipment in the wiring closet, and the wall plate in the office. This provides 10 meters of cable allowance to accommodate patch cables at each end of the link, signal losses in intermediate wire terminations on the link, etc. Woodward recommends halving these maximum distances for use in industrial environments.

### Shielding

Double shielded Ethernet cable must be used between the AtlasPC control and any other devices. Standard Ethernet cables used in office environments are NOT shielded. Unshielded cables will very likely lead to communication problems and unreliable control operation.

The shield must always be AC-coupled at one end and connected directly to earth on the opposite end for proper operation. The Atlas has been constructed so that the Ethernet cable shield is AC-coupled to earth at the Atlas. It is assumed that most other devices on the network will provide for direct grounding of the shield at that device. However, if an external device provides AC-coupling of its shield, Woodward can supply an Ethernet Interface FTM (Field Termination Module) to allow earth grounding at the Atlas end of the cable. The FTM (part number 5453-754) has two female RJ45 connectors. One is AC-coupled to its chassis, and the other is direct coupled to its chassis.

### **Slave Hardware**

Woodward is always testing new Ethernet networked Distributed I/O modules. When an Ethernet interface module has been proven to meet Woodward's requirements, it will be documented in this section.

### **Software for Application Developers**

	It is possible to disrupt an existing Ethernet network by attaching an improperly configured device. To prevent problems on your existing Ethernet network, read this chapter before connecting the AtlasPC Ethernet ports to a network.
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IMPORTANT	Many end users will be purchasing pre-programmed AtlasPC units and will not need the information in this section. The information below is aimed at programmers using the GAP programming tool provided by Woodward. The information provided here covers the basics. For more detail, refer to Woodward software manual 26103, <i>Woodward NT Real Time Operating System Service and Interface Tools</i> or software manual 26199, <i>Woodward VxWorks Real Time Operating System</i> .
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Programmers will need the following:

- GAP<sup>™</sup> Programming Tool 3.03 or later to create the application. (This can be downloaded from our website: **www.woodward.com/ic/software**)
- For more information on these and additional software tools mentioned in this chapter, see Woodward software manual 26103 (NT RTOS) or 26199 (VxWorks RTOS).

### IP Address Setup

The AtlasPC Ethernet connections are designed to work with either DHCP servers or with fixed IP addresses.

## IMPORTANT

DHCP systems work by automatically detecting and assigning an IP address for some fixed amount of time, often known as a "lease". If a unit is given a lease and then sits offline for a period of time longer than the lease, then it becomes necessary to put the unit back on to a DHCP network in order to reconnect to the unit. For this reason, all AtlasPC systems ship with fixed addresses to prevent problems for customers who do not use DHCP systems.

- Refer to the software tools manual (26103 or 26199) for factory default IP address settings and configuration details.
- If two or more AtlasPC controls are to be used on the same network, the IP addresses must be changed to *unique* addresses (valid for your particular network) or to DHCP mode, whichever is appropriate in order to avoid address conflicts.
- AppManager can be used to view the AtlasPC Ethernet ports' existing IP addresses. To find the 2nd Ethernet port's IP address, connect to the Ethernet port, highlight the unit's name in AppManager, and press the "Control Info" button. Under "Footprint Description"→ "Network Adaptors" there should be two IP addresses. One is the AtlasPC Ethernet IP; the other is the AtlasPC PC/104 Ethernet IP.

 The PC/104 Ethernet connection must be configured with a different network domain identifier from the primary Ethernet connection resident on the CPU board. If this is not done, the operating system will only require one port to operate even though both may respond to ping requests.

# NOTICE

Whether you use DHCP or fixed address networks, you must configure all AtlasPC units, and to ensure proper operation of both ports, they must be on different domains. Refer to the Woodward software manual supplied with your control for further details.

### Ethernet Software Configuration – (GAP)

- Program the Ethernet ports in the GAP Application. There can be multiple UDP ports assigned by using several UDP\_P GAP blocks. Each UDP\_P output can connected to a PORT\_x input in a MODBUS\_S or MODBUS\_M block.
- Load and execute the GAP application. GAP will initialize the Ethernet ports with the Configuration data and acquire the I/O information.

#### TCP/IP

- Use the FBUS\_M block in the GAP application. No port is needed. Multiple FBUS\_M blocks can be used.
- Load and execute the GAP application.

### Chapter 4. Serial (Modbus) Interface

### Introduction

This chapter has been divided into two sections, Hardware for End Users, and Software for Application Developers. The hardware section is aimed at customers that are applying the Atlas in a permanent installation. The software section is for customers that are developing software for the AtlasPC<sup>™</sup> control.

The AtlasPC control uses AEG-Modicon Inc.'s Modbus protocol. The Modbus protocol determines how the master and slaves establish and break off contact, how the sender and receiver are identified, how messages are exchanged in an orderly manner, and how errors are detected. The protocol also controls the query and response cycle which takes place between the master and slave devices.

### Serial Software and Hardware Requirements

- GAP Programming Tool (all versions)
- Serial cables and connectors
- Slave Interface and Modules
- Device Memory Maps and Scaling (Manuals)
- Woodward Interface Tools

### Hardware for End Users

### Serial (Modbus) Port Protocols

There are up to five serial communication ports on the Atlas platform that may be used for the Modbus interface. Modbus can use RS-232, RS-422, and RS-485 configurations. The one or two communication ports on the CPU board are fixed as RS-232, and are non-isolated. Shielded cables and Serial Port Isolator/ Converter(s) are required when using these ports. The first two ports on the SmartCore board may be configured for RS-232, RS-422, or RS-485, and the last port is configurable for RS-232 only.

**RS232**—An ANSI (American National Standards Institute) standard definition of electrical, functional, and mechanical connections for communications between DTE (Data Terminal Equipment) and DCE (Data Communications Equipment) such as connection of a computer to a modern. It has gained wide usage in short distance applications (15 m/50 ft). In practice the standard is largely ignored beyond the most rudimentary implementation of electrical signals (±3 to ±15 volts). Woodward's implementation will support speeds up to 115K baud in AtlasPC systems. The actual specification allows 19.2K baud at up to 15 m (50 ft).

**RS422**—Also an ANSI standard definition of electrical connections for communications between devices. Because it uses balanced drivers, it can communicate over long distances (1200 m/4000 ft) at high baud rates (115K). Woodward's implementation of RS-422 is actually a 4-wire RS-485 communications network. Since Woodward convention has been to call this RS-422, this manual will continue to do so. However, it may be important to understand that the actual port is RS-485. The port supports up to 32 devices as a full duplex, multi-drop communications network. This allows more than one device to be connected to the common bus with a single master requesting data. It requires two twisted pairs and ground to operate.

**RS485**—Also an ANSI standard definition of electrical connections for communications between devices. Because it uses balanced drivers, it can communicate over long distances (1200 m/4000 ft) at high baud rates (115K). This protocol is implemented identically to "RS-422" with the exception that only one twisted pair is required. Both transmitted and received data use the same pair of wires. A ground wire is still required since the output is isolated. The port supports up to 32 devices as a half duplex, multi-drop communications network. This allows more than one device to be connected to the common bus with a single master requesting data. It requires one twisted pair and ground to operate.

### **Interface Cables and Connectors**

When choosing a cable for RS-485, it is necessary to examine the required distance of the cable and the data rate of the system. Beyond the obvious traits such as number of conductors and wire gauge, cable specifications include a handful of less intuitive terms.

**Characteristic Impedance (ohms)**—A value based on the inherent conductance, resistance, capacitance, and inductance of a cable that represents the impedance of an infinitely long cable. When the cable is cut to any length and terminated with this Characteristic Impedance, measurements of the cable will be identical to values obtained from the infinite length cable. Therefore, termination of the cable with this impedance gives the cable the appearance of being infinite length, allowing no reflections of the transmitted signal. When termination is required in a system, the termination impedance value should match the Characteristic Impedance of the cable.

**Shunt Capacitance (pF/ft)**—The amount of equivalent capacitive load of the cable, typically listed in a per foot basis (1 pF/ft = 3.28 pF/m). One of the factors limiting total cable length is the capacitive load. Systems with long lengths benefit from using low capacitance cable.

**Propagation velocity (% of c)**—The speed at which an electrical signal travels in the cable. The value given typically must be multiplied by the speed of light (c,  $3x10^8$  m/s) to obtain units of meters per second. For example, a cable that lists a propagation velocity of 67% gives a velocity of 0.67 x  $3x10^8 = 2.01x10^8$  m/s. The higher the percentage, the smaller the signal delay.

General recommendations for serial cable are listed in the following table.

Impedance:	100 Ω ±20%	
Cable capacitance:	52.5 pF/m (15.0 pF/ft) at 1 kHz	
Propagation Velocity:	67.0%	
Data Pairs;	0.2 mm <sup>2</sup> (24 AWG) solid bare copper	
Signal attenuation:	6.0 dB maximum	

### **Recommended Bulk Cable**

For simplicity, Woodward will recommend cables consistent with long cable lengths and high baud rates. Longer cable lengths may be possible at lower baud rates with the best cables but are not supported by the ANSI standards for RS-485. The same cables may be used for RS-232 applications, but length will be limited to 15 m (50 ft).

Ethernet Category 5 cable is a very good cable selection for RS-485 networks. It will support cables lengths to 1200 m (4000 ft) at baud rates up to 115,200. Since Ethernet cable is easy to find and is inexpensive, it will often be the cable of choice. Always use shielded cable.

Installations with high electrical interference (noise) and/or long cable lengths together with high baud rates may benefit from larger gauge cable.

### **Network Construction**

While there are a number of different ways to physically connect devices on a network, Woodward recommends that multi-drop networks be constructed using a "daisy chain" configuration or a "backbone with stubs" for best performance. In a daisy chain, wires are run from device one to device two to device three, etc. In a backbone with stubs, a main trunk line is run between the two devices that are physically farthest apart, and then stub lines are run from the intermediate devices to the trunk line. Stubs should be kept as short as possible. See Volume I, Figure 11-2 for a graphical representation.

### Termination

To achieve best performance with RS-485 serial communication networks, it is necessary to terminate the network to prevent interference caused by signal reflections. RS-232 networks are short enough that termination is not required. For ease of setup, Woodward has provided built-in network termination resistors on the SmartCore board for the RS-485 serial ports. To activate the termination resistors, an external jumper must be placed at the connector. The resistor network used is a special design intended to provide maximum noise immunity. The same design should be used at the opposite end of the network. This termination network is necessary due to limitations of the Modbus protocol. (See the information in the SmartCore chapters of Volume I.)

Termination resistors must be installed only on the two units that are at the physical ends of the network. Terminating other midpoint units can overload the network and put it into a cyclic thermal shutdown mode. As a rule, no matter how many units are on a network, there should never be more than two terminations installed. For 2-wire networks, a termination network should be used at the two physical ends of the network. For 4-wire networks, Woodward has elected to use a termination network only across the receiver lines at either end of the network. This is feasible due to the baud rate limit of 115K. In either case (2- or 4-wire configurations), a total of two termination networks are used.

### Shielding

Shielded cable is required between the AtlasPC control and any other devices. Unshielded cables and improperly shielded cables are likely to cause communication problems and unreliable control operation. The shield must always be ac-coupled (connected through a capacitor) at one end and connected directly to earth on the opposite end for proper operation. The SmartCore board has been constructed so that the serial port Shield connections are directly connected to the Atlas chassis ground (which must be tied directly to earth). Devices connected to the opposite end of the cable must provide for the accoupled shield connection.

Woodward has found that a 0.01  $\mu$ F capacitance is typically adequate for this purpose. A minimum rating of 1000 Vdc on the capacitor is required.

Connector	Terminal	Signal Mnemonic
PHOENIX	SmartCore	
00000000000	with	
	Actuator Pinout	
1	93	232 TXD
2	94	232 RXD
3	95	SIG GND
4	96	422/485 (+) RECEIVE
5	97	TERM RES. +
6	98	TERM RES
7	99	422/485 (–) RECEIVE
8	100	422 (+) TRANSMIT
9	101	422 (1) TRANSMIT
10	102	SHLD (CHASSIS)

#### Connectors Pinouts SmartCore SIO # 1 Connector and Pinout

SmartCore SIO # 2 Connector and Pinout

Connector	Terminal	Signal Mnemonic
PHOENIX	SmartCore	
0000000000	with	
	Actuator Pinout	
1	83	232 TXD
2	84	232 RXD
3	85	SIG GND
4	86	422/485 (+) RECEIVE
5	87	TERM RES. +
6	88	TERM RES
7	89	422/485 (–) RECEIVE
8	90	422 (+) TRANSMIT
9	91	422 (1) TRANSMIT
10	92	SHLD (CHASSIS)

### SmartCore SIO # 3 Connector and Pinout

Connector	Signal Mnemonic
DB9F	Shielded DB9 female receptacle
5 1 ••••• ••••• ••••	
1	
2	RXD
3	TXD
4	
5	GND
6	
7	
8	
9	
Shield	

### **CPU Comm 1 Connector and Pinout**

Connector	Signal Mnemonic
DB9F	Shielded DB9 female receptacle
1	DCD
2	RXD
3	TXD
4	DTR
5	SIG COM.
6	DSR
7	RTS
8	CTS
9	RI
Shield	SHLD (CHASSIS)

### CPU Comm 2 Connector and Pinout

Connector	Signal Mnemonic
DB9F	Shielded DB9 female receptacle
1	DCD
2	RXD
3	TXD
4	DTR
5	SIG COM.
6	DSR
7	RTS
8	CTS
9	RI
Shield	SHLD (CHASSIS)

### **Network Wiring**

See Chapters 5 and 6 of Volume I for serial I/O wiring.

### **Network Length**

When choosing a transmission line for RS-232, RS-422, or RS-485, it is necessary to examine the required distance of the cable and the data rate of the system. Losses in a transmission line are a combination of AC losses (skin effect), dc conductor loss, leakage, and AC losses in the dielectric.

Maximum Distances	
RS-232	15 m (50 ft)
RS-422, RS-485	1219 m (4000 ft)

### Serial (Modbus) Slave Hardware

The AtlasPC control system may control Modbus slave modules from many different manufacturers. With the exception of Woodward-manufactured devices, Woodward makes no expressed or implied statement of suitability of these devices. It is the user's responsibility to ensure EMC compliance of their system, if necessary, by using distributed modules that are CE compliant. The following Serial Modbus slave hardware has been tested with the AtlasPC control to confirm functionality.

1) All Woodward devices designed for Modbus.

2) Allen-Bradley F	Flex I/O
Part Number	Description
3170-MBS	I/O Network Interface for Modbus (Slave) (ProSoft Technologies)
1794-IB16	Discrete Input (Sink)
1794-OV16	Discrete Output (Sink)
1794-OW8	Discrete Output (Relay)
1794-IE8/B	Analog Input (Current)
1794-OE4/B	Analog Output (Current)
1794-IT8	Thermocouple Input
1794-CJC2	Cold Junction
1794-IR8	RTD Input
1794-TB3S	Terminal Base
1794-TB3TS	Terminal Base

Woodward

3) Automation Direct Terminator I/O		
Part Number	Description	
Part Number T1K-01AC	Description Power Supply	
Part Number T1K-01AC T1K-01DC	Description Power Supply Power Supply	
Part Number T1K-01AC T1K-01DC T1K-MODBUS	Description Power Supply Power Supply Modbus Interface	
Part Number T1K-01AC T1K-01DC T1K-MODBUS T1K-08ND3	Description Power Supply Power Supply Modbus Interface Discrete Input (Sink)	
Part Number     T1K-01AC     T1K-01DC     T1K-MODBUS     T1K-08ND3     T1K-16ND3	Description Power Supply Power Supply Modbus Interface Discrete Input (Sink) Discrete Input (Sink)	
Part Number     T1K-01AC     T1K-01DC     T1K-MODBUS     T1K-08ND3     T1K-16ND3     T1K-16TD1	Description   Power Supply   Power Supply   Modbus Interface   Discrete Input (Sink)   Discrete Output	
Part Number     T1K-01AC     T1K-01DC     T1K-08ND3     T1K-16ND3     T1K-16TD1     T1K-08TRS	Description   Power Supply   Power Supply   Modbus Interface   Discrete Input (Sink)   Discrete Output   Discrete Output (Relay)	
Part Number     T1K-01AC     T1K-01DC     T1K-MODBUS     T1K-08ND3     T1K-16ND3     T1K-16TD1     T1K-08TRS     T1F-16AD-1	Description   Power Supply   Power Supply   Modbus Interface   Discrete Input (Sink)   Discrete Output   Discrete Output   Discrete Output (Relay)   Analog Input (Current)	
Part Number     T1K-01AC     T1K-01DC     T1K-MODBUS     T1K-08ND3     T1K-16ND3     T1K-16TD1     T1K-08TRS     T1F-16AD-1     T1F-16DA-1	Description   Power Supply   Power Supply   Modbus Interface   Discrete Input (Sink)   Discrete Output (Sink)   Discrete Output   Discrete Output (Relay)   Analog Input (Current)   Analog Output (Current)	
Part Number     T1K-01AC     T1K-01DC     T1K-MODBUS     T1K-16ND3     T1K-16ND3     T1K-16TD1     T1K-08TRS     T1F-16AD-1     T1F-16DA-1     T1F-14THM	Description   Power Supply   Power Supply   Modbus Interface   Discrete Input (Sink)   Discrete Output (Sink)   Discrete Output   Discrete Output (Relay)   Analog Input (Current)   Analog Output (Current)   Thermocouple Input	
Part Number     T1K-01AC     T1K-01DC     T1K-MODBUS     T1K-16ND3     T1K-16TD1     T1K-08TRS     T1F-16AD-1     T1F-16DA-1     T1F-14THM     T1K-08B-1	Description   Power Supply   Power Supply   Modbus Interface   Discrete Input (Sink)   Discrete Output (Sink)   Discrete Output   Discrete Output (Relay)   Analog Input (Current)   Analog Output (Current)   Thermocouple Input   Terminal Base	

### **Software for Application Developers**

#### Many end users will be purchasing pre-programmed AtlasPC units **IMPORTANT** and will not need the information in this section. The information below is aimed at programmers using the GAP programming tool provided by Woodward. The information provided here covers the basics. For more detail, refer to Woodward software manual 26103, Woodward NT Real Time Operating System Service and Interface Tools or software manual 26199, Woodward VxWorks Real Time Operating System.

Programmers will need the following:

- Device memory maps and scaling (Manuals) •
- GAP<sup>™</sup> Programming Tool (all versions) to create the application. (This can be downloaded from our website: www.woodward.com/ic/software)
- For more information on these and additional software tools mentioned in this chapter, see Woodward software manual 26103 (NT RTOS) or 26199 (VxWorks RTOS).

The AtlasPC control is configured to communicate with a Serial network by performing the following steps:

- Determine slave and I/O modules to be used. 1.
- Determine order of I/O modules. 2.
- Review the Serial Modbus slave manuals and understand the hardware 3. addressing.
- 4. Create GAP application which reads and writes to the Serial I/O.
- 5. Transfer GAP application to AtlasPC control.
- 6. Start GAP application.

### Serial (Modbus) Software Configuration (Protocol)

The AtlasPC control supports both the ASCII and RTU versions of the Modbus protocol. RTU is more widely used since it is the more efficient of the two.

- ASCII: hex coding / 7 bits per character (4 transmitted) / any parity / 1 or 2 stop bits
- RTU: 8 bit binary coding/ 8 bits per char (8 transmitted) / any parity / 1 or 2 stop bits

RTU sends data in 8-bit binary characters. ASCII firsts divides each RTU character into two 4-bit parts (high order and low order) and then represents them by their hexadecimal equivalent. The ASCII characters representing the hexadecimal characters are used to construct the message thus using twice as many characters as RTU mode. Additionally, RTU message characters are transmitted in a continuous stream, whereas ASCII can have breaks of up to one second between characters.

The following is a guideline for configuring a serial port interface from the control to a communication device.

	Modbus RTU
BAUD	10 (38400)
BITS	2 (RTU-8 bits)
STOP	1 (1 stop)
PARITY	1 (none)
MODE	1 (line)
FLOW	1 (off)
ECHO	1 (off)
ENDLINE	3 (crlf)
IGNCR	1 (off)

#### Serial (Modbus) Software Configuration (GAP)

See the Distributed I/O Examples later in this chapter for specific configuration examples for Allen-Bradley and Automation Direct applications.

After completing the GAP application, it must be compiled and downloaded to the AtlasPC control's PC using AppManager. Once the GAP application is started on the AtlasPC control's PC, the Serial Modbus module will automatically initialize and start the Modbus Network.

## IMPORTANT

The timing of the serial scan rate will depend on the number of groups (heads) and the number of nodes (I/O modules) in the network and will be independent of the rate group structure.

## Chapter 5. PC104 CanOpen Interface



CanOpen is a protocol that uses CAN (Controller Area Network). Currently, Woodward is developing the AtlasPC<sup>™</sup> CanOpen interface module, and will document its use in this chapter in the near future.

### Chapter 6. Distributed I/O Examples

### Introduction

This chapter documents the hardware setup and software configuration for two manufacturers of Distributed I/O modules. Since there are numerous manufacturers and options available by numerous manufacturers, Woodward chose Allen-Bradley Flex I/O as a representative of a high end Distributed I/O system and Automation Direct Terminator I/O hardware as a low cost system representative. There are other good high end and low cost manufactures of Distributed I/O systems and therefore these examples should not be taken as a Woodward endorsement. The I/O configurations for each manufacturer were limited to specific I/O modules and a limited application of the possible options available with these modules.

It is the responsibility of the end user to review the options available from each distributed I/O supplier and derive the necessary software configurations needed to support their specific applications. Woodward Governor Company makes no expressed or implied statement of suitability for the Allen-Bradley, Automation Direct, or any other supplier of Distributed I/O systems. It is hoped that these specific examples of I/O module configurations can be used as a foundation for building a majority of the AtlasPC control applications where Distributed I/O is needed. Ease in applying the Woodward software interface may differ from vendor to vendor. Due to limited resources, Woodward can only supply limited technical support for those applications using other vendors or part numbers not shown in these examples. If extensive support is required, contact Woodward for setting up an application development contract.

At this writing, both Allen-Bradley and Automation Direct have Profibus, DeviceNet, and Modbus Interface Modules that are compatible with the AtlasPC interfaces. Both Allen-Bradley and Automation Direct have an Ethernet Interface Module, but neither module is presently compatible with the AtlasPC interface.

The following examples will demonstrate a step-by-step process to use in generating a distributed I/O network.

### Implementing a Distributed I/O Network

- 1. Determine the number and type of I/O channels needed.
- 2. Select the desired network protocol (Profibus, DeviceNet, Modbus, etc.).
- 3. Select the best manufacturer of I/O modules that meet the network and I/O requirements.
- 4. Layout the hardware configuration (how the modules will be arranged and wired).
- 5. Create the Applicom configuration files or Modbus addressing configuration.
- 6. Generate an address spreadsheet to track address numbers for Reads and Writes based on the specific module memory maps and/or the GSD or EDS files for Profibus and DeviceNet respectively.
- 7. Review the published documentation on the I/O modules and select the options required.
- 8. Generate the GAP I/O files.
- 9. Wire control and Distributed I/O network.
- 10. Download the GAP and Applicom files into the control.
- 11. Run application and verify functionality.

### Allen-Bradley Flex I/O Example

In this example, a specific set of Allen-Bradley Flex I/O hardware was selected to represent a typical distributed I/O system. Three different network interfaces are shown. In this example, a Profibus, DeviceNet, and Modbus interface head is connected to the I/O module string to demonstrate these three types of setups.

All three network interfaces use the same I/O module configuration and order. The Profibus and Modbus Network interface modules are manufactured by a third party manufacturer (ProSoft Technology, Inc.). Allen-Bradley manufactures the DeviceNet module.

Quantity	Module	Manuf. P/N
1 ea	Discrete Input (Sink)	1794-IB16
1 ea	Discrete Output (Sink)	1794-OV16
1 ea	Discrete Output (Relay)	1794-OW8
1 ea	Analog Input (Current)	1794-IE8/B
1 ea	Analog Output (Current)	1794-OE4/B
1 ea	Thermocouple Input	1794-IT8
1 ea	Cold Junction	1794-CJC2
1 ea	RTD Input	1794-IR8
6 ea	Terminal Base	1794-TB3S
1 ea	Terminal Base	1794-TB3TS
1 ea	Profibus Interface	3170-PDP
1 ea	DeviceNet interface	1794-ADM
1 ea	Modbus Interface	3170-MBS

### Allen-Bradley Flex I/O Profibus Configuration

Each Allen-Bradley FLEX I/O module requires a terminal base that snaps onto a DIN rail to the right of the previous I/O module. Each I/O module is then plugged into its own terminal base. Terminal bases make up a modular backplane for 1794 FLEX I/O modules and make up a modular terminal block for I/O connections. Each terminal base provides a backplane connection between the network interface adapter module and I/O modules.

In this example, one 3170-PDP PROFIBUS adapter is interfaced with seven terminal base units with installed FLEX I/O modules, forming a FLEX I/O system. A maximum of eight I/O modules may be connected to one interface module.

The 3170-PDP is a Network Interface Adapter that communicates between the FLEX I/O module backplane and AtlasPC/Master across the PROFIBUS DP network. The 3170-PDP module is a slave device to the AtlasPC control, and is a master controller of the FLEX I/O modules. The I/O data exchange occurs as follows: Output data is sent from the AtlasPC control across the PROFIBUS DP network to the 3170-PDP adapter. The network interface adapter then automatically transfers the data across the FLEX I/O backplane to the output modules. Inputs from the input modules are collected by the network interface adapter via the backplane and sent across the PROFIBUS DP network to the AtlasPC control.

In order to simplify the nomenclature used in creating the GAP application, certain naming conventions were changed with respect to the manufacturer's naming convention. In this example, Woodward refers to the node address as the Group address. The 3170-PDP node address (Group address), is set by using the 2–position thumbwheel switch. In this example the address is set to 01. Use a pen to press either the + or – buttons to change the number.

Upon power-up, the 3170-PDP goes to an initialization state and performs a selftest (memory check, data memory clear). If a failure occurs, the interface adapter transitions to a faulted state and waits for reset (cycle power). Otherwise, the adapter begins monitoring the network (run state) for messages.

In this example, the power wiring is daisy–chained to the Network Interface adapter and then to the terminal bases. See Figure 6-1 for Allen-Bradley Flex I/O configuration layout.



Figure 6-1. Allen-Bradley Flex I/O Configuration

#### Address Spreadsheet

The I/O map for a module is divided into read words and write words. Read words consist of input and status words, and write words consist of output and configuration words. The number of read words or writes words can be 0 or more.

In this example, the first read word received by the AtlasPC control from the Network Interface Adapter (3170-PDP) is the Adapter Status Word. This is followed by the input data from each Node, in the order of the installed I/O modules. The Input data from Node 1 is first after the status word, followed by Input data from Node 2, and so on up to slot 7. The Output data is received by the Network Interface Adapter in the order of the installed I/O modules. The Output data for Node 1 is received first, followed by the Output data for Node 2, and so on up to slot 7. All bits in the adapter write word are reserved and therefore are not used by the GAP application.

To keep track of the addressing for all of the reads and write addresses, the creation of an address spreadsheet is very useful. This address spreadsheet can be derived from the GSD file supplied by the manufacturer of the network interface module (head).

The GSD file defines how the network interface module interacts with the I/O modules being used. The GSD file can be downloaded from the Internet at the network interface module manufacturer's site. It needs to be imported into the Applicom configuration program to create the necessary configuration files.

#### **Applicom Setup Procedure**

- 1. In ApplicomIO Console, select Description, Add Board.
- 2. Select Diagnostic and Manual Configuration.
- 3. Select PC104/ISA and PC104\_DPIO.
- 4. Set the IRQ to 5.
- 5. Select OK.
- 6. Select Library, Add. Locate the ProSoft GSD file, psft0882.gsd.

## IMPORTANT

This PSFT0882.GSD file is used by ApplicomIO tool to help set up the system. The ApplicomIO configuration tool automatically reads the PSFT0882.GSD file and extracts defaults used in the data exchange. The GSD file is in ASCII format and can be viewed with any text editor.

- 7. 7) Open ProSoft Technology Inc and select 3170-PDP.
- 8. 8) Select Library, Insert in Configuration. In the Modules Configuration tab, select and add each module in the Profibus string, including the adapter and any empty slots, and verify that they are listed in the correct order. This tells how many input and output bytes are allocated to each module. In the GSD file, there are two types of configurations for each type of module (condensed and full format).

## IMPORTANT

When setting up the ApplicomIO configuration, the Big Endian and Little Endian option reverses the order of the bytes in a word for the Analog reads and writes. Big Endian is high byte first. Always use the Big Endian option. Doesn't apply to discrete read and write words.

## IMPORTANT

The condensed configuration does not use all reads and writes for all of the modules as seen in the full format configuration and on the Memory Map tables shown in the manufactures documentation. In this example, the condensed configuration was used for setting up the addressing spreadsheet. Verify the number of reads and writes for each module in GSD file. Configure the required reads and writes in the spreadsheet accordingly.

Addressing is sequential starting with the slave network interface module, which gets the first read word and the first write word. The rest are addressed according to how many read words and write words are associated with each module, and in what order the modules are installed. Addressing begins at 0, not 1. For example, an IB16 module has one read and one write word, and the OV16 module has two write words. When configuring a slave interface module with one IB16 module followed by one OV16 module, the slave interface module is assigned read bits 0 through 15 (one word) and write bits 0 through 15 (one word), the IB16 module gets read bits 16 through 31 (one word) and write bits 32 through 63 (two words).

Based on the GSD file, the address spreadsheet can be calculated. Using the configuration of the example, the following address spreadsheet was generated. See Table 6-1 for the address spreadsheet.

After creation of the address spreadsheet, the functionality associated with these addresses must be obtained. This is done by reviewing the documentation for each module supplied by the manufacturer.

# 

The number of read and write addresses between the documented Memory Map and the GSD file may not always agree. When creating the address spreadsheet, always allocate the number of addresses specified in the GSD file.

Use the following documents from the manufacturer to obtain the Memory Maps and related information.

### Module

Discrete Input (Sink)
Discrete Output (Sink)
Discrete Output (Relay)
Analog Input (Current)
Analog Output (Current)
Thermocouple Input
RTD Input
Profibus Interface

**Document P/N** 1794-5.4 1794-5.29 1794-5.19 1794-5.6 1794-5.5 1794-6.5.7 1794-6.5.4 FLEX-UM-PDP-1.2

Module	Word #	<b>Read Address Bits</b>	Write Address Bits
3170-PDP	0	0-15	0-15
1794-IB16	0	16-31	16-31
1794-OV16	0	None	32-47
	1		48-63
1794-OW8	0	None	64-79
1794-IE8/B	0	32-47	80-95
	1	48-63	
	2	64-79	
	3	80-95	
	4	96-111	
	5	112-127	
	6	128-143	
	7	144-159	
	8	160-175	
1794-OE4/B	0	176-191	96-111
	1		112-127
	2		128-143
	3		144-159
	4		160-175
	5		176-191
1794-IT8	0	192-207	192-207
	1	208-223	208-223
	2	224-239	224-239
	3	240-255	240-255
	4	256-271	
	5	272-287	
	6	288-303	
	7	304-319	
	8	320-335	
	9	336-351	
	10	352-367	
1794-IR8	0	368-383	256-271
	1	384-399	272-287
	2	400-415	288-303
	3	416-431	
	4	432-447	
	5	448-463	
	6	464-479	
	7	480-495	
	8	496-511	
	9	512-527	
	10	528-543	

Table 6-1. Profibus Bit Address Spreadsheet

#### **GAP** Application

When setting up a new GAP application, create the chassis block with the appropriate network interface configuration for the AtlasPC control chosen. In Figure 6-2, an Applicom Profibus Master Network interface adapter is located in slot 6 and an Applicom Master DeviceNet Network interface adapter in slot 7. The DeviceNet slot is not used in this example, but will be used in the DeviceNet example (see Allen-Bradley Flex I/O DeviceNet Configuration below).



Figure 6-2. AtlasPC Chassis GAP Block

When creating a new GAP application, the Applicom Profibus module is defined with the FB\_MODULE hardware block from the FieldBus MODULES menu. It is generated automatically when "Generate channel sheet(s)" is chosen in the chassis configuration. If more than one Profibus network interface module is going to be connected to the A6 interface, then use the Append Rpt button to create additional IO\_B\_X input fields within the FB\_MODULE block. See Figure 6-3 for example of FB\_MODULE with two Profibus interface groups. Only one interface group is used in the following example.



Figure 6-3. Example of GAP Application FB\_Module

The next GAP block that connects to the FB\_MODULE block is the FB\_EQUIP block. This block can be found under the Hardware Group, select the FB\_MODULES tab and then select the FB\_EQUIP block. This block is used to define the Profibus network interface adapter. Use the Append Rpt button to create additional IO\_B\_X fields within the FB\_EQUIP block. Every FB I/O block used for this distributed I/O group needs an IO\_B\_X field. If there are many I/O blocks, as in this example, the FB\_EQUIP block. IO\_B\_X fields can't all be displayed on a single FB\_EQUIP block. To simplify the block, only the first channel for each node is shown. All other input channels are hidden. See Figure 6-4 for FB\_EQUIP setup example.



Figure 6-4. FB\_EQUIP Block Example

The COMM\_ERR output goes TRUE if there is a Communications error from the PC104 Profibus Master to the individual Profibus Slave. The ERR\_NUM output displays the error number to define the type of error the Profibus slave has detected (See Table 12.7.1.1-2, Applicom Error Num Table Definition). It has been found that if there is a loss of communications between the Profibus master and slave occurs, the COMM\_ERR will go true and ERR\_NUM will be 33. The COMM\_ERR will remain true until communications is restored.

Error	Definition
0	No anomaly detected. The function took place correctly.
1	Unknown function. The requested function is not supported.
2	Incorrect address. The address of the variable you are soliciting is incorrect.
3	Incorrect data. Further details :Profibus DP protocol :- Wrong initialization of the parameters related to the configuration of the equipment - Start the configuration
	again and import the GSD file.
4	Irretrievable data.
6	Layer 2 negative acknowledgment from the equipment (NACK).Further details :Profibus DP protocol:- NO (Not Ok) , remote equipment is missing or defective.
10	Layer 2 negative acknowledgment from the equipment (NACK). Further details :Protocol Profibus:- UE (User Error), Error in remote equipment.
11	Layer 2 negative acknowledgment from the equipment (NACK).Profibus Protocol:- RR (Remote Resource), Not enough resources in remote equipment. Or invalid initialization parameters.
12	Layer 2 negative acknowledgment from the equipment (NACK).Further details :Profibus Protocol:- RS (Remote Service), The layer 2 service used is not authorized on the SAP or the SAP is not activated.
13	Layer 2 negative acknowledgment from the equipment (NACK).Further details :Profibus Protocol:- RDL (Response FDL/FMA1/2 Data Low), Not enough resources in remote equipment to reply in low priority.
14	Layer 2 negative acknowledgment from the equipment (NACK).Further details :Profibus Protocol:- RDH (Response FDL/FMA1/2 Data High), Not enough resources in remote equipment to reply in high priority. Or invalid initialization parameters.
15	Profibus Protocol:- LS (Local Service), local SAP not activated.
16	Profibus Protocol:- NO (Not OK), Significance dependent on layer 2 service.
21	Profibus Protocol:- IV (Invalid parameter in request),Further details : TS ApplicomIO® = adr equipment. TS or adr equipment > to HSA
32	Bad parameter passed into the function. Incorrect number of variables.
33	Response time fault (Time-Out).Further details :- The remote equipment is missing- the data of the local slave DP is not polled by another master.
36	Equipment not configured. Define the equipment configuration with PCCONFIO and start again the ApplicomIO® product.

Table 6-2. Applicom Error Num Table Definition

There are two approaches to configuring the I/O blocks (FB\_BI, FB\_BO, FB\_AI, and FB\_AO). One way would be to use one block and use the repeat option to create multiple fields within the block. This approach was used in this example to read status bits (FB\_BI) such as underrange, overrange, etc. and to set functions (FB\_BO) such as filter times, ranges, etc. The other way to configure the application would be to use an I/O block for every channel or every bit. This approach was used to create individual channels. Alternatively, FB\_INITA and FB\_INITB blocks could be used for writes that only need to occur on power-up. In this example, the FB\_INITA and FB\_INITB blocks are not used.

### Nomenclature

When creating a new GAP application, it is important to establish a well organized block naming convention up front. Once done, it is easier to find specific functions and I/O within a large GAP application. In this example, Woodward has formulated certain nomenclature rules to facilitate ease in navigating through the example application. Here are some rules to follow:

- 1. The AtlasPC control is always referred to as the A1 Chassis. If there were more than one AtlasPC control per system, then they would be A2, A3, etc.
- The board slots in the AtlasPC control are referred to as slots A01 A07. The Profibus slot is A06 and the DeviceNet slot is A07 in this example.
- 3. The Profibus network may consist of one or more network interface adapters, (3170-PDP). Each adapter (referred to as Nodes by Allen-Bradley) and its associated modules are listed as groups G1, G2, etc.
- 4. A group may consist of one to eight I/O modules. These modules (referred to as slots by Allen-Bradley) are listed as nodes N1\_, N2\_, etc., followed by the module type.
- 5. To designate status and config. blocks, Read or Write followed by a 1, 2, or 3 is used to delineate individual words written or read from a module.
- 6. A period is used to separate the category, block name, and block field nomenclature.
- In the table below, a GAP block that has a single channel per block is referred to as a configuration type 1. These blocks are named with Category = G1Nx\_xxxx, Block name = BI\_01, BI\_02, etc. or BO\_01, BO\_02, etc.
- A GAP block that has multiple bits per block is referred to as a configuration type 2. These blocks are named with Category = G1Nx\_xxx, Block name = READ1, READ2, etc. or WRITE1, WRITE2, etc.

For this example, the naming convention has been setup as follows.

Module Type	Block Type	Nomenclature	<b>Configuration Type</b>
All	FB MODULE	A1.A06 PB	N/A
All	FB_EQUIP	A06 PB.GROUP1	N/A
IB16 (Read)	FB BI	G1N1 IB16.BI 01, 02, 0	etc. 1
IB16 (Write)	FB_BO	G1N1 IB16.WRITE	2
OV16 (Write)	FB_BO	G1N2 OV16.BO 01, 02	2, etc. 1
OW8 (Write)	FB_BO	G1N3_OW8.BO_1, 2, e	tc. 1
IE8/B (Read)	FB_BI	G1N4_IE8/B.READ	2
IE8/B (Write)	FB_BO	G1N4_IE8/B.WRITE	2
IE8/B (Read)	FB_AI	G1N4_IE8/B.AI_1, 2, et	c. 1
OE4/B (Read)	FB_BI	G1N5_OE4/B.READ	2
OE4/B (Write)	FB_BO	G1N5_OE4/B.WRITE1	2
OE4/B (Write)	FB_BO	G1N5_OE4/B.WRITE2	2
OE4/B (Write)	FB_AO	G1N5_OE4/B.AO_1, 2,	etc. 1
IT8 (Read)	FB_BI	G1N6_IT8.READ1	2
IT8 (Read)	FB_BI	G1N6_IT8.READ2	2
IT8 (Write)	FB_BO	G1N6_IT8.WRITE1	2
IT8 (Write)	FB_BO	G1N6_IT8.WRITE2	2
IT8 (Write)	FB_BO	G1N6_IT8.WRITE3	2
IT8 (Read)	FB_AI	G1N6_IT8.TC_1, 2, etc.	. 1
IR8 (Read)	FB_BI	G1N7_IR8.READ1	2
IR8 (Read)	FB_BI	G1N7_IR8.READ2	2
IR8 (Write)	FB_BO	G1N7_IR8.WRITE1	2
IR8 (Write)	FB_BO	G1N7_IR8.WRITE2	2
IR8 (Write)	FB_BO	G1N7_IR8.WRITE3	2
IR8 (Read)	FB_AI	G1N7_IR8.RTD_1, 2, e	tc. 1

1 Single channel per block (Single Repeat) 2 Multiple bits per block (Multiple Repeat)

### AtlasPC Digital Control, Vol. II (Distributed I/O)

From the GSD file, the number of read and write addresses and their order were defined based on the physical order of the modules and the memory maps defined by Allen-Bradley. The GAP application is also constructed in the same order that the modules are ordered. In setting up the first I/O module in GAP, the application must read and write to the specific addresses defined in the address spreadsheet. These read and write addresses are used to extract data from the distributed I/O modules and to set certain options. In GAP, reads are done with FB\_AI and FB\_BI blocks, writes with FB\_AO and FB\_BO blocks. Al's and AO's are addressed by the byte, while BI's and BO's are addressed by the bit. The following steps will show how to set up these FB\_XX blocks to read and write to the distributed I/O modules.

## IMPORTANT

Allen-Bradley modules reverse the order of the high and low bytes of their discrete reads and writes (BI's and BO's). this has to be accommodated in the BI and BO GAP blocks as shown in Table 6-3.

Spreadsheet	FB_BI Address	FB_BO Address	FB_BI	FB_BO Input
Address #	Field	Field	Output Field	Field
8	BI_ADD_1	BO_ADD_1	BI_V_1	BO_V_1
9	BI_ADD_2	BO_ADD_2	BI_V_2	BO_V_2
10	BI ADD 3	BO ADD 3	BIV 3	BOV3
11	BI ADD 4	BO ADD 4	BIV4	BOV4
12	BI ADD 5	BO ADD 5	BIV 5	BOV5
13	BI_ADD_6	BO_ADD_6	BI_V_6	BO_V_6
14	BI_ADD_7	BO_ADD_7	BI_V_7	BO_V_7
15	BI_ADD_8	BO_ADD_8	BI_V_8	BO_V_8
0	BI ADD 9	BO ADD 9	BIV 9	BO V 9
1	BI ADD 10	BO ADD 10	BI V 10	BO V 10
2	BI ADD 11	BO ADD 11	BI V 11	BO V 11
3	BI_ADD_12	BO_ADD_12	BI_V_12	BO_V_12
4	BI_ADD_13	BO_ADD_13	BI_V_13	BO_V_13
5	BI_ADD_14	BO_ADD_14	BI_V_14	BO_V_14
6	BI_ADD_15	BO_ADD_15	BI_V_15	BO_V_15
7	BI ADD 16	BO ADD 16	BI V 16	BO V 16

See Table 6-3 for example of Boolean address order for block field numbering.

Table 6-3. Example of Boolean Address Order

### ProSoft Network Interface Adapter (3170-PDP) Module



Based on the address spreadsheet, the ProSoft Network Interface Adapter 3170-PDP has one read and one write address word allocated in the memory map. According to the FLEX-UM-PDP-1.2 User Manual from ProSoft, the write word is reserved. Therefore there is no need to write to addresses 0-15. See Figure 18-5. for the read memory map for the 3170-PDP Interface Module.

Bit Description	Bit	Explanation
I/O Module Fault	8	This bit is set (1) when an error is detected in slot position 1.
	9	This bit is set (1) when an error is detected in slot position 2.
	10	This bit is set (1) when an error is detected in slot position 3.
	11	This bit is set (1) when an error is detected in slot position 4.
	12	This bit is set (1) when an error is detected in slot position 5.
	13	This bit is set (1) when an error is detected in slot position 6.
	14	This bit is set (1) when an error is detected in slot position 7.
	15	This bit is set (1) when an error is detected in slot position 8.
Reserved	1-7	Reserved
Node Address Changed	0	This bit is set (1) when the node address switch setting has been changed since power up.

### Memory Map

Figure 6-5. 3170-PDP Network Interface Memory Map

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The node address (Group address) changed bit is set when the node address switch setting has been changed since power up. The new node address does not take affect until the adapter has been powered down and then powered back up. Until this power cycling occurs, the node address switches will not match the actual node address.

Based on this memory map, an FB\_BI read block was created to allow the GAP application to read all of the used bits. See Figure 6-6 for example of setup of STATUSREAD GAP block used to read the 3170-PDP memory map.



Figure 6-6. Example of 3170-PDP Memory Map Read GAP Block

### Allen-Bradley 24 Vdc Sink Input (1794-IB16) Module



In this example, the 1794-IB16 module is plugged into a 1794-TB3S base. See Figure 6-7 for example of 1794-IB16 module wiring.

DIST Allen-Bradle	RIBUTED I/O y FLEX I/O 1794-IB1		To 24VDC Com	
DISC	RETE INPUT			To +24VDC
	(-COM)	B16		
	(+24VDC)	C34	_	_
	DI (+)	A0		
PBI.A1.A06.G1.N1_BI_01	(-COM)	B17	2	
	(+24VDC)	C35	_	
	DI (+)	A1	 3	
PBI.A1.A06.G1.N1_BI_02	(-COM)	B18		
	(+24VDC)	C36	_	
	DI (+)	A2		
PBI.A1.A06.G1.N1_BI_03	(-COM)	B19		
	(+24VDC)	037	_	
	DI (+)	A3	5	
PBI.A1.A06.G1.N1_BI_04	(-COM)	B20		
	(+24VDC)	0.38		
	DI (+)	A4		
PBI.A1.A06.G1.N1_BI_05	(-COM)	B21		
	(+24VDC)	0.39	_	
		A3	7	
PDI.A1.A00.G1.N1_DI_00	(-COM)	622		
	(+24VDC)	040	8	
PRI 41 406 G1 N1 BL 07	(-COM)	B23	-	
	(+24)/DC)	C41		
	DI (+)	A7		
PBI.A1.A06.G1.N1 BI 08	(-COM)	B24	8	
1 01.71.700.01.141_01_00	(+24VDC)	C42		
	DI (+)	A8	10	
PBLA1.A06.G1.N1 BL 09	(-COM)	B25		_
	(+24VDC)	C43		
	DI (+)	A9	1	
PBI.A1.A06.G1.N1 BI 10	(-COM)	B26		
	(+24VDC)	C44		
	DI (+)	A10	 1:	
PBI.A1.A06.G1.N1_BI_11	(-COM)	B27		_
	(+24VDC)	C45		
	DI (+)	A11	 1:	
PBI.A1.A06.G1.N1_BI_12	(-COM)	B28		_
	(+24VDC)	C46		
	DI (+)	A12	 1	
PBI.A1.A06.G1.N1_BI_13	(-COM)	B29		
	(+24VDC)	C47		/
	DI (+)	A13		
PBI.A1.A06.G1.N1_BI_14	(-COM)	B30		
	(+24VDC)	C48		
	DI (+)	A14	10	
PBI.A1.A06.G1.N1_BI_15	(-COM)	B31		
	(+24VDC)	C49		
	DI (+)	A15	 1	
PBI.A1.A06.G1.N1_BI_16	(-COM)	B32		
	(+24VDC)	C50		
	(-COM)	B33		
	(+24VDC)	C51		

Figure 6-7. Example of 1794-IB16 Module Wiring

The memory map indicates that there are two read addresses and one write address. The condensed format used to set up the address spreadsheet only uses one read and one write address. See Figure 6-8 for memory map of Allen-Bradley 1794-IB16 Discrete input module.

### Memory Map

Dec.	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Read 0	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
Read 1	C = 16 bit Counter Value of Input 15															
Write	N us	ot ed	CF	CR	Not used				FT 12–15			FT 00–11				
Where: D C FT CI CI NOTE: C, Ac	Where: D = Data Input - 0 = input off, 1 = input on   C = Counter value for input 15   FT = Input Filter Time   CR = Counter Reset   CF = Counter Fast - where 1 = Fast Input (raw) data, 0 = Standard Input filtered data   NOTE: C, CR and CF not available when used with any series 1794-ASB or 1794-ASB2 Remote I/O   Adapter Modules															

Figure 6-8. 1794-IB16 Memory Map

In this example, this module was set up with filter times of 256us for all inputs, Counter Reset set to off, and Counter set to standard input filtered data. See Figure 6-9 for input filter time bit map and Figure 6-10 for example of 1794-IB16 Write GAP block.

#### **Input Filter Times**

Bits			Description	Colostad			
02	01	00	Filter Time for Inputs 00–11(00–13)	Selected Filter Time			
05	04	03	Filter Time for Inputs 12–15(14–17)	The Thic			
0	0	0	Filter Time 0 (default)	256µs			
0	0	1	Filter Time 1	512µs			
0	1	0	Filter Time 2	1ms			
0	1	1	Filter Time 3	2ms			
1	0	0	Filter Time 4	4ms			
1	0	1	Filter Time 5	8ms			
1	1	0	Filter Time 6	16ms			
1	1	1	Filter Time 7	32ms			

Figure 6-9. 1794-IB16 Input Filter Time Bit Map





To read the discrete input bits for the 1794-IB16 module, individual FB\_BI blocks were used. See Figure 6-11 for example of GAP block configuration.



Figure 6-11. Example of 1794-IB16 Discrete Input Read GAP Blocks

### AtlasPC Digital Control, Vol. II (Distributed I/O)

Each of the FB\_BI blocks have fault indication (BI\_F\_X) and fault number (BI\_FN\_X) output fields for each channel within the block. In this example there is only one channel per block and the BI\_FN\_X field is hidden. These fault fields may be used during initial application checkout to identify programming errors. The BI\_F\_X and BI\_FN\_X fields display the same errors as the COMM\_ERR and ERR\_NUM fields in the FB\_EQUIP block. Therefore, only the FB\_EQUIP COMM\_ERR and ERR\_NUM fields need to be monitored for faults after the application and hardware has been verified to work. The FB\_BO, FB\_AI, and FB\_AO blocks also have similar fault output fields and can be treated the same as the FB\_BI block fields. The BI\_R\_X field is used to reset the fault output fields. By setting TRUE on the BI\_R\_1 input, the fault output is non-latching.



### Allen-Bradley 24 Vdc Sink Output (1794-OV16) Module

In this example, the 1794-OV16 is connected to a Woodward 16 channel relay module. See Figure 6-12 for example of 1794-OV16 module wiring.

			+28VDC	TB49 +
DIS	TRIBUTED I/O		28COM	TB50 -
Allen-Bradle	ey FLEX I/O 1794-OV1	6	J1-23	Woodward
			J1-24	40 Observal Dalau
DISC	REIEOUIPUI	<b>D</b> 40	J1-21	To Channel Relay
	(+24)/DC)	B16		P/N 5441-691
	(+24VDC)	0.04	J1-19	K1 OF
BBLA1 406 C1 N2 BO 01	DO (+)	R17		P/N 5441-419
100000000000000000000000000000000000000	(+24VDC)	C35		
	DO (+)	A1	J1-18	K2
PBI.A1.A06.G1.N2 BO 02	(-COM)	B18		112
	(+24VDC)	C36		
	DO (+)	A2	J1-17	K3
PBI.A1.A06.G1.N2_BO_03	(-COM)	B19		K5
	(+24VDC)	C37		
	DO (+)	A3	J1-16	KA
PBI.A1.A06.G1.N2_BO_0	(-COM)	B20		14
	(+24VDC)	C38	14 45	
	DO (+)	A4	31-13	K5
PBI.A1.A06.G1.N2_BO_05	(-COM)	B21		
	(+24VDC)	C39	.11-14	1/0
	DO (+)	A5	0114	KG
PBI.A1.A06.G1.N2_BO_06	(-COM)	BZZ		
	(+24VDC)	C40	J1-13	
BBI 61 605 C1 N2 BO 07	DO (+)	R0 R23		K/
PBIX1.00.01.142_B0_07	(+24)/DC)	C41		
	(124700) DO (+)	Δ7	J1-12	K8
PRI A1 A06 G1 N2 BO 08	(-COM)	B24		
	(+24VDC)	C42		
	DO (+)	A8	J1-11	К9
PBLA1.A06.G1.N2_BO_09	(-COM)	B25		
	(+24VDC)	C43		
	DO (+)	A9	J1-10	K10
PBI.A1.A06.G1.N2_BO_10	(-COM)	B26		
	(+24VDC)	C44	14.0	K11
	DO (+)	A10	31-9	KII
PBI.A1.A06.G1.N2_BO_11	(-COM)	B27		
	(+24VDC)	C45	.11-8	K12
	DO (+)	A11		K1Z
PBLA1.A06.G1.N2_BO_12	(+24)/DC)	D20		
	(+24VDC)	A12	J1-7	K13
PBI 41 405 C1 N2 BO 13	(+COM)	B29		
1000100.01112_00_10	(+24VDC)	C47		
	DO (t)	A13	J1-6	K14
PBLA1.A06.G1.N2_BO_1	(-COM)	B30		K14
	(+24VDC)	C48		
	DO (+)	A14	J1-5	K15
PBI.A1.A06.G1.N2_B0_15	(-COM)	B31		NI3
	(+24VDC)	C49		1440
	DO (+)	A15	J1-4	K10
PBLA1.A06.G1.N2_BO_16	(-COM)	B32		
	(+24VDC)	C50		
	(-COM)	B33	To 24VDC	сом
L	(+24VDC)	C51	► 10 +24VD	U C

Figure 6-12. Example of 1794-OV16 Module Wiring

The memory map indicates that there are zero read addresses and one write address. The condensed format used to set up the address spreadsheet specifies zero read and two write addresses. The extra write word is not defined in the memory map therefore no GAP block is used. However this undefined address must be reserved when setting up the address spreadsheet. See Figure 6-13 for memory map of 1794-OV16 module.

#### **Memory Mapping**

Bit⇒ Word <b></b> ↓	15	14	13	12	11	10	09	80	07	06	05	04	03	02	01	00
Read	Not used															
Write	015	014	O13	012	011	O10	09	08	07	06	O5	04	O3	02	01	00
Where:	Where: O = Output value															

Figure 6-13. 1794-OV16 Module Memory Map

To write the discrete output bits for the 1794-OV16 module, individual FB\_BO blocks were used. See Figure 6-14 for example of GAP write block configuration.



Figure 6-14. Example of 1794-OV16 GAP Write Blocks

Allen-Bradley Relay Output (1794-OW8) Module


In this example, the relay outputs are individually fused to protect the module. See Figure 6-15 for example of 1794-OW8 module wiring.



Figure 6-15. Example of 1794-OW8 Module Wiring

The memory map indicates that there are one read address and one write address. The condensed format used to set up the address spreadsheet specifies zero read and one write address. Since the read address is not used, nothing is read from this address for this example. See Figure 6-16 for memory map of 1794-OW8 module.

# Image Table Memory Map

Word	'	Memo Maj	ory o	Dec. Bits (Octal Bits)					Description					Format				
Read		Inpu	ıt	00-	15 (00	)–17)	N	ot usec	l – res	erved								
Write		Outp	ut		00–0	7	R ci ci	Relay Output data – 00 corresponds to output 0, 01 corresponds to output 1, etc.						0 = Output off 1 = Output on				
				-80	15 (10	)–17)	Ν	Not used										
Dec.	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00		
(Octal)	17	16	15	14	13	12	11	11 10 07 06 05 04						02	01	00		
Write			No	t used	- set i	io 0			07	06	05	04	03	02	01	00		

Where O = Output number

When bit = 0, output is off; when bit =1, output is on

Figure 6-16. 1794-OW8 Module Memory Map

To write the discrete output bits for the 1794-OW8 module, individual FB\_BO blocks were used. See Figure 6-17 for example of GAP write block configuration.



Figure 6-17. Example of 1794-OW8 GAP Write Blocks

# Allen-Bradley Analog Input (1794-IE8/B) Module



In this example, loop powered transducers are shown. See Figure 6-18 for example of 1794-IE8/B module wiring.



Figure 6-18. Example of 1794-IE8/B Module Wiring

The memory map indicates that there are nine read addresses and one write address. The condensed format used to set up the address spreadsheet specifies the same. See Figure 6-19 for the input memory map and Figure 6-20 for the output memory map for the 1794-IE8/B module.

# Input Map

Bit⇒ Word	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
↓																
							R	ead								
0	S					A	nalog	Input '	Value	for Ch	annel	0				
1	S		Analog Input Value for Channel 1													
2	S		Analog Input Value for Channel 2													
3	S		Analog Input Value for Channel 3													
4	S		Analog Input Value for Channel 4													
5	S					A	nalog	Input '	Value	for Ch	annel	5				
6	S					A	nalog	Input '	Value	for Ch	annel	6				
7	S					A	nalog	Input '	Value	for Ch	annel	7				
8	PU		Not used - set to 0         U7         U6         U5         U4         U3         U2         U1         U0													
Where:	S = S U = I PU =	Sign bi Underi = Powe	ign bit (in 2's complement) Inderrange bits Power up bit													

Figure 6-19. 1794-IE8/B Input Module Memory Map

**Underrange bits (U)**—These bits are set (1) when the input channel is below a preset limit as defined by the configuration selected. U0 (bit 00) corresponds to input channel 0 and U1 (bit 01) corresponds to input channel 1, etc.

**Power Up (unconfigured state) bit (PU)**—This bit is set (1) when the configuration word is all zeroes (0) due to a reset (adapter power cycle or module insertion) or a cleared configuration word (all 0). When this bit is set (1), the module status indicator flashes.

#### Output Map

Bit⇒ Word∜	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Write															
0	C7	C6	C5	C4	C3	C2	C1	C0	F7	F6	F5	F4	F3	F2	F1	F0
Where:	C = Configure select bit = Full rance bit															

#### **Range Selection Bits**

•																
Channel No.	Ch	. 0	Ch	. 1	Ch	<b>.</b> 2	Ch	. 3	Ch	. 4	Ch	. 5	Ch	. 6	Ch	. 7
	F0	C0	F1	C1	F2	C2	F3	C3	F4	C4	F5	C5	F6	C6	F7	C7
Decimal Bits	00	08	01	09	02	10	03	11	04	12	05	13	06	14	07	15
0-10V dc/0-20mA	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
4–20mA	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
-10 to +10V dc	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Off <sup>1</sup>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C = Configure select bit																

F = Full range bit

<sup>1</sup> When configured to Off, individual input channels will return 0000H.

Figure 6-20. 1794-IE8/B Output Module Memory Map

In this example, this write block is set up with Range Select bits for all channels set to 0-21mA. The read block is set up to be able to read the status of the underrange bits for all channels and the Power Up bit (PU). See Figure 6-21 for example of 1794-IE8/B Read and Write GAP blocks.



Figure 6-21. Example of 1794-IE8/B Read and Write GAP Blocks

To read the analog input words for the 1794-IE8/B module, individual FB\_AI blocks were used. The addressing for the analog input blocks needs to be in bytes rather than bits. To convert from spreadsheet bit addresses to bytes, take the first bit of the word in the spreadsheet for the 1794-IE8/B module and divide by 8bits/byte (32÷8=4). Repeat this calculation for the rest of the addresses for each channel. The relationship between raw counts and engineering units needs to be specified in the analog read block. The raw count to milliamp relationship can be found in the Allen-Bradley manual 1794-6.5.2. See Figure 6-22 for Analog Data Format Table. The table specifies counts in Hexadecimal form and the FB\_AI block requires the AI\_RL\_1 and AI\_RH\_1 fields to be entered in decimal form. Under the 0-20mA column in the Analog Data Format Table, 21mA is equivalent to 7FF8 Hexadecimal. Converting 7FF8 to decimal equals 32760 Counts High. In this example the block was scaled to 0-21mA (engineering units) for 0-32760 counts from the module. See Figure 6-23 for example of 1794-IE8/B GAP Analog Read Blocks.

Current (m A)	4 00mA Mada	0 20mA Mada	Voltone (10	+10 Vol	t Mode	0-10 Volt
Current (mA)	4-20mA Mode	U-ZUMA Mode	voitage (v)	Input	Output	Mode
			-10.50	8000	8000	
0.00		0000	-10.00	8620	8618	
1.00		0618	-9.00	9250	9248	
2.00		0C30	-8.00	9E80	9E78	
3.00		1248	-7.00	AAB0	AAA8	
4.00	0000	1860	-6.00	B6E0	B6D8	
5.00	0787	1E78	-5.00	C310	C310	
6.00	0F0F	2490	-4.00	CF40	CF40	
7.00	1696	2AA8	-3.00	DB70	DB70	
8.00	1E1E	30C0	-2.00	E7A0	E7A0	
9.00	25A5	36D8	-1.00	F3D0	F3D0	
10.00	2D2D	3CF0	0.00	0000	0000	0000
11.00	34B4	4310	1.00	0C30	0C30	0C30
12.00	3C3C	4928	2.00	1860	1860	1860
13.00	43C3	4F40	3.00	2490	2490	2490
14.00	4B4B	5558	4.00	30C0	30C0	30C0
15.00	52D2	5B70	5.00	3CF0	3CF0	3CF0
16.00	5A5A	6188	6.00	4920	4928	4928
17.00	61E1	67A0	7.00	5550	5558	5558
18.00	6969	6DB8	8.00	6180	6188	6188
19.00	70F0	73D0	9.00	6DB0	6DB8	6DB8
20.00	7878	79E8	10.00	79E0	79E8	79E8
21.00	7FFF	7FF8	10.50	7FF0	7FF8	7FF8







# Allen-Bradley Analog Output (1794-OE4/B) Module



See Figure 6-24 for example of 1794-OE4/B module wiring.





### AtlasPC Digital Control, Vol. II (Distributed I/O)

The memory map indicates that there is one read address and 13 write addresses. The condensed format used to set up the address spreadsheet specifies one read address and 6 write addresses. From the output memory map addresses 6-9 are not used and 10-13 are used to specify safe state values that are not available in the condensed format. Therefore, the output memory map words 0-5 correspond to the six write words specified in the address spreadsheet. See Figure 6-25 for the input memory map and Figure 6-26 for the output memory map for the 1794-OE4/B module.

#### Input Map

**Output Map** 



Figure 6-25. 1794-OE4/B Module Input Memory Map

#### Bit⇒ Word↓ 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00 0 S Analog Data – Channel 0 S Analog Data – Channel 1 1 2 Analog Data – Channel 2 S S Analog Data – Channel 3 3 Μ Μ Μ Μ 4 Not used - set to 0 2 3 0 1 Not used - set to 0 C3 C2 C1 C0 Not used - set to 0 F3 F2 F0 5 F1 6-9 Not used - set to 0 10 S Safe state value for channel 0 11 S Safe state value for channel 1 12 S Safe state value for channel 2 13 S Safe state value for channel 3 Where: S = Sign bit (in 2's complement) M = Multiplex control bit C = Configure select bit F = Full range bit

Figure 6-26. 1794-OE4/B Module Output Memory Map

Multiplex control bit (M) for individual channels. These bits control the safe state analog outputs. – Bit 00 corresponds to output channel 0, bit 01 corresponds to output channel 1, and so on.

1 = use words 0,1,2 or 3 as directed by channel number n.

0 = use words 10, 11, 12 or 13 as directed by channel number n.

For definition of Fx and Cx bits, see Figure 6-27.

Channel No.	Cł	n. O	Ch	n. 1	Cł	ı. 2	Ch	ı. 3				
	F0	C0	F1	C1	F2	C2	F3	C3				
Decimal Bits	00	08	01	09	02	10	03	11				
0-10V dc/0-20mA	1	0	1	0	1	0	1	0				
4–20mA	0	1	0	1	0	1	0	1				
-10 to +10V dc	1	1	1	1	1	1	1	1				
Off <sup>1</sup> 0 0 0 0 0 0 0												

Figure 6-27.	1794-OE4/B	Write Range	Selection Bits
--------------	------------	-------------	----------------

In this example, the read block is set up to monitor the four broken wire addresses and the power up bit on the module. The write blocks are set up to configure the module for multiplex control and 0-20mA range. Since word addresses 10-13 are not defined with the condensed format in the GSD file, the multiplex control functionality is not relevant. Therefore all of the M bits were set to true. See Figure 6-28 for example of 1794-OE4/B Read and Write GAP blocks.





# AtlasPC Digital Control, Vol. II (Distributed I/O)

To write the analog output words for the 1794-OE4/B module, individual FB AO blocks were used. The addressing for the analog output blocks needs to be in bytes like the analog input blocks. To convert from spreadsheet bit addresses to bytes, take the first bit of the word in the spreadsheet for the 1794-OE4/B module and divide by 8 bits/byte (96+8=12). Repeat this calculation for the rest of the addresses for each channel. For the 1794-OE4/B module to output the correct current, the GAP block must convert the engineering units requested to raw counts used by the module. The milliamp to raw count relationship can be found in the Allen-Bradley manual 1794-6.5.2. See Figure 6-22 for Analog Data Format Table. The table specifies counts in Hexadecimal form and the FB AO block requires the AO\_RL\_1 and AO\_RH\_1 fields to be entered in decimal form. Under the 0-20mA column, of the Analog Data Format Table, 21mA is equivalent to 7FF8 Hexadecimal and 0mA is 0000 Hexadecimal. Converting 7FF8 to decimal equals 32760 Counts High. In this example the block was scaled to 0-21mA (engineering units) for 0-32760 counts from the module. See Figure 6-29 for example of 1794-OE4/B GAP Analog Write Blocks.



Figure 6-29. Example of 1794-OE4/B GAP Analog Write Blocks

NOTICE

An AO requires a limiter on the input value to keep it from exceeding the 21 mA value. Values above 21 mA will roll back over to zero.

# Allen-Bradley Thermocouple Input (1794-IT8) Module



In this example, the first six channels are used for thermocouples and the last two channels are used for monitoring the reference junction temperatures. See Figure 6-30 for example of 1794-IT8 module wiring.



Figure 6-30. Example of 1794-IT8 Module Wiring

### AtlasPC Digital Control, Vol. II (Distributed I/O)

The memory map indicates that there are eleven read addresses and 3 write address. The condensed format used to set up the address spreadsheet specifies eleven read addresses and 4 write addresses. The extra write word is not defined in the memory map, therefore no GAP block is used. However this undefined address must be reserved when setting up the address spreadsheet. In this example the undefined write address was allocated to addresses 240 through 255. See Figure 6-31 for the input memory map and Figures 6-32 through 6-35 for the output memory map for the 1794-IT8 module.

Thermocoup	hermocouple/mV Input Module (1794-IT8) Read															
Decimal Bit	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Octal Bit	17	16	15	14	13	12	11	10	07	06	05	04	03	02	01	00
Read Word 0									Reserve	ed						
1								Chan	nel O Inp	out Data	l					
2		Channel 1 Input Data														
3		Channel 2 Input Data														
4		Channel 3 Input Data														
5		Channel 4 Input Data														
6								Chan	nel 5 Inp	out Data	ı					
7								Chan	nel 6 Ing	out Data	l					
8								Chan	nel 7 Ing	out Data	ı					
9				Overra	ange B	its						Under	range B	its		
10	0	0	0	0	0	Bad Cal	Cal Done	Cal Range	0	Diag	gnostic S	tatus	Pwr Up	Bad Structure	CJC over	CJC Under

Figure 6-31. 1794-IT8 Module Input Memory Map

**Underrange bits**—These bits are set if the input signal is below the input channel's minimum range.

**Overrange bits**—These bits are set if 1) the input signal is above the input channel's maximum range, or 2) an open detector is detected.

**Cold Junction sensor underrange bit**—This bit is set if the cold junction temperature is below 0 °C.

**Cold Junction sensor overrange bit**—This bit is set if the cold junction temperature is above 70 °C.

**Bad Structure**—This bit is set if an invalid thermocouple type is selected. **Powerup bit**—This bit is set (1) until configuration data is received by the module.

**Critical Error bits**—If these bits are anything other than all zeroes, return the module to the factory for repair.

**Calibration Range bit**—Set to 1 if a reference signal is out of range during calibration

**Calibration Done bit**—Set to 1 after an initiated calibration cycle is complete. **Calibration Bad bit**—Set to 1 if the channel has not had a valid calibration.

Thermocouple/	mv.	Inermocouple/mv input Module (1/94-118) write														
Dec. Bit	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Octal Bit	17	7 16 15 14 13 12 11 1							07	06	05	04	03	02	01	00
Write Word 0		8-Bit Calibration Mask							Cal Clk	Cal hi Cal lo	F	ilter Cuto	ff	FDF	Data	Туре
1	Ther	Thermocouple 3 Type Thermocouple 2 Type							Thermocouple 1 Type Thermocouple 0					ole 0 Typ	e	
2	2 Thermocouple 7 Type Thermocouple 6 Typ					уре	Т	'hermoco	uple 5 Ty	уре	Th	ermocoup	ole 4 Typ	e		
Where: EDE - fixed	tinital filt	or hit														

Thermocouple/mV Input Module (1794-IT8) Write

Figure 6-32. 1794-IT8 Module Output Memory Map

Word	Decimal Bit (Octal Bit)					Description										
Write Word 0	00-01 (00-01)	Module	e Data T	ype												
		Bit	01	00	Definit	ion										
			0	0	°C (de	fault)										
			0	1	٥F											
			1	0	Bipolar	counts scaled between -32768 and +32767										
			1	1	Unipola	ar counts scaled between 0 and 65535										
	Bit 02 (02)	Fixed 1 100% ( Defau	ixed Digital Filter - When this bit is set (1), a software digital filter is enabled. This filter settles to 00% of a Full Scale step input in 60 times the selected first notch filter time shown on page 4-3. Jefault - filter disabled.) JD Filter First Notch Frequency													
	03-05 (03-05)	A/D Fil	A/D Filter First Notch Frequency													
		Bit	05	04	04         03         Definition           0         0         10Hz (default)           0         1         25Hz											
			0	0												
			0	0												
			0	1	0	50Hz										
			0	1	1	60Hz										
			1	0	0	100Hz										
			1	0	1	250Hz										
			1	1	0	500Hz										
		1 1 1 1000hZ														
	06 (06)	Calibra	tion Hig	h/Low bi	t – This	bit is set during gain calibration; reset during offset calibration.										
	07 (07)	Calibra calibrat	tion cloo tion.	k - this	bit must	be set to 1 to prepare for a calibration cycle; then reset to 0 to initiate										
	08-15 (10-17)	Calibra corresp	tion mas conds to	sk – The channel	channe 0, bit 9	I, or channels, to be calibrated will have the correct mask bit set. Bit 8 to channel 1, and so on.										

Figure 6-33. 1794-IT8 Write Word 0

#### Hardware First Notch Filter

A/D Filter First Notch Frequency (effective resolution)	10Hz (16-bits)	25Hz (16-bits)	50Hz (16-bits)	60Hz (16-bits)	100Hz (16-bits)	250Hz (13-bits)	500Hz (11-bits)	1000Hz (9-bits)
Number of channels scanned			Sys	tem Throughp	out (in ms an	d s)		
1	325	145	85	75	55	37	31	28
2	650	290	170	150	110	74	62	56
3	975	435	255	225	165	111	93	84
4	1.3s	580	340	300	220	148	124	112
5	1.625s	725	425	375	275	185	155	140
6	1.95s	870	510	450	330	222	186	168
7	2.275s	1.015s	595	525	385	259	217	196
8	2.60s <sup>1</sup>	1.16s	680	600	440	296	248	224
1 Default setting								

Figure 6-34. 1794-IT8 Hardware First Notch Filter

Word	Decimal Bit (Octal Bit)					Description
Write Word 2	00-03 (00-03)	Channel 0	Thermocou	ple Type		
		Bit 0	3 02	01	00	Thermocouple Type – Range
		0	0 0	0	0	Millivolts (default)
		0	) 0	0	1	B 300 to 1800°C (572 to 3272°F)
		0	) 0	1	0	E -270 to 1000°C (-454 to 1832°F)
		0	) 0	1	1	J -210 to 1200°C (-346 to 2192°F)
		0	) 1	0	0	K -71 to 1372°C (-95 to 2502°F)
		0	) 1	0	1	R -50 to 1768°C (-58 to 3214°F)
		0	) 1	1	0	S -50 to 1768°C (-58 to 3214°F)
		0	) 1	1	1	T -73 to 400°C (-99 to 752°F)
		1	0	0	0	C 0 to 2315°C (32 to 4199°F)
		1	0	0	1	N -270 to 1300°C (-450 to 2372°F)
		1	0	1	0	Reserved
		1	0	1	1	Reserved
		1	1	0	0	Module reports cold junction temperature for channels 00-03
		1	1	0	1	Module reports cold junction temperature for channels 04-07
		1	1	1	0	Reserved
		1	1	1	1	No sensor connected (do not scan)
	04-07 (04-07)	Channel 1	Thermocou	ple Type	(see bit	s 00-03)
	08-11 (10-13)	Channel 2	Thermocou	ple Type	(see bit	s 00-03)
	12-15 (14-17)	Channel 3	Thermocou	ple Type	(see bit	s 00-03)
Write Word 3	00-03 (00-03)	Channel 4	Thermocou	ple Type	(see wri	ite word 2, bits 00-03)
	04-07 (04-07)	Channel 5	Thermocou	ple Type	(see wri	ite word 2, bits 00-03)
	08-11 (10-13)	Channel 6	Thermocou	ple Type	(see wri	ite word 2, bits 00-03)
	12-15 (14-17)	Channel 7	Thermocou	ple Type	(see wri	ite word 2, bits 00-03)

Figure 6-35. 1794-IT8 Write Word 1 and 2 (Note: Write Words 2 & 3 should be labeled 1 & 2)

In this example, the first read block is set up to monitor the all of the under and overrange bits on the module. The second read block monitors the Cold Junction sensor underrange bit, Cold Junction sensor overrange bit, Bad Structure, Powerup bit, Critical Error bits, Calibration Range bit, Calibration Done bit, and Calibration Bad bit. The first write word(1) sets the module for °F units, 100 Hz filtering, and no calibration. The second write word(2) sets the module for type K thermocouples on channels 0, 1, 2, and 3. The third write word(3) sets the module for type K thermocouples for channels 4 and 5, cold junction (0-3) temperature on channel 6, and cold junction (4-7) on channel 7. See Figure 6-36 for GAP read and write block example.

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	G1N6 IT	18		G1N6 IT8 READ2		G1N6 ITS		G1N6 IT8 WRITE2		G1N6 IT8 WRITE3	
(A1/6/G1/N6/TC)-	IO_CHANNE	L	(AI/8/G1/N6/TC)-	IO_CHANNEL	*TRUE	B0_V_1	*FALSE	B0_V_1	"FALSE	B0_V_1	
CH1 UNDERRANGE-	BI_C_1	BI_V_16	COLD JUNCTION UNDERRANGE -	BI_C_1 BI_V_1	*FALSE-	B0_V_2	-(_A1/6/G1/N6/TC_) *FALSE-	BO_V_2	-( <u>A1/6/G1/N6/TC</u> ) *FALSE-	B0_V_2	-(_A1/6/G1/N6/TC_
CH2 UNDERRANGE-	BI_C_2	BI_V_2≽	COLD JUNCTION OVERRANGE -	BI_C_2	*FALSE-	B0_V_3	*TRUE-	B0_V_3	*TRUE-	B0_V_3	
CH3 UNDERRANGE-	BL_C_3	BI_V_3P	INVALID TO TYPE -	BI_C_3	*FALSE-	B0_V_4	*FALSE-	B0_V_4	*FALSE-	B0_V_4	
CH4 UNDERRANGE-	BI_C_4	BI_V_45	POWER UP BIT -	BI_C_4	"FALSE-	B0_V_6	*FALSE-	BO_V_5	"FALSE-	B0_V_5	
CH5 UNDERRANGE-	BI_C_5	BI_V_65	CRITICAL ERROR BITS -	BI_C_6	*TRUE-	B0_V_6	*FALSE-	BO_V_6	*FALSE*	B0_V_6	
CH6 UNDERRANGE-	BL_C_6	BI_V_65	CRITICAL ERROR BIT -	BI_C_6	*FALSE-	B0_V_7	*TRUE-	B0_V_7	*TRUE-	B0_V_7	
CH7 UNDERRANGE-	BLC_7	BI_V_7>	CRITICAL ERROR BIT -	BI_C_7	*FALSE-	B0_V_8	*FALSE-	B0_V_8	*FALSE-	B0_V_8	
CH8 UNDERRANGE-	BI_C_8	BI_V_8>	NOT USED -	BI_C_8 BI_V_9	*FALSE-	B0_V_9	*FALSE-	BO_V_9	*FALSE-	BO_V_9	
CH1 0VERRANGE-	BI_C_9	BI_^_0b	OUT OF RANGE DURING CALIBRATION -	BI_C_9	*FALSE-	BO_V_10	*FALSE-	BO_V_10	*FALSE-	B0_V_10	
CH2 OVERRANGE-	BI_C_10		CALIBRATION DONE -	BI_C_10	*FALSE-	B0_V_11	*TRUE-	B0_V_11	*TRUE-	B0_V_11	
CH3 OVERRANGE-	BI_C_11		CALIBRATION BAD -	BI_C_11	*FALSE-	B0_V_12	*FALSE-	B0_V_12	*TRUE-	B0_V_12	
CH4 0VERRANGE-	BI_C_12	LV_129	NOT USED -	BI_C_12	*FALSE-	B0_V_13	*FALSE-	BO_V_13	*TRUE-	B0_V_13	
CH5 0VERRANGE-	BI_C_13	LV_139	NOT USED -	BI_C_13	*FALSE-	B0_V_14	*FALSE-	B0_V_14	*FALSE-	B0_V_14	
CH6 OVERRANGE-	BI_C_14		NOT USED -	BI_C_14	*FALSE-	B0_V_15	*TRUE-	B0_V_15	*TRUE-	B0_V_15	
CH7 OVERRANGE-	BI_C_15	1_V_15P	NOT USED -	BI_C_15	*FALSE-	B0_V_16	*FALSE-	BO_V_16	*TRUE-	B0_V_16	
CH8 OVERRANGE-	BI_C_16	1_0_160	NOT USED -	BI_C_16	200 —	BO_ADD_1	216 -	BO_ADD_1	232 -	BO_ADD_1	
344 -	BI_ADD_1		360 -	BI_ADD_1	201 -	BO_ADD_2	217 -	BO_ADD_2	233 -	BO_ADD_2	
345 -	BI_ADD_2		361 -	BI_ADD_2	202 —	BO_ADD_3	218 -	BO_ADD_3	234 -	B0_ADD_3	
346 -	BI_ADD_3		362 -	BI_ADD_3	203 —	BO_ADD_4	219 —	BO_ADD_4	235 -	BO_ADD_4	
347 -	BI_ADD_4		363 -	BI_ADD_4	204	BO_ADD_6	220	BO_ADD_6	236 -	BO_ADD_5	
348 -	BI_ADD_6		364 -	BI_ADD_5	205 —	BO_ADD_6	221 -	BO_ADD_6	237 -	BO_ADD_6	
349 -	BI_ADD_6		365 -	BI_ADD_6	206 —	BO_ADD_7	222 -	BO_ADD_7	238 -	B0_ADD_7	
350 -	BI_ADD_7		366 -	BI_ADD_7	207 —	BO_ADD_8	223 -	BO_ADD_8	239 -	BO_ADD_8	
351 -	BI_ADD_8		367 -	BI_ADD_8	192 —	BO_ADD_9	208 —	BO_ADD_9	224 -	BO_ADD_9	
336 -	9LADD_9		362 -	BI_ADD_9	193 —	B0_ADD_10	209 —	BO_ADD_10	225 -	B0_ADD_10	
337 -	BI_ADD_10		353 -	BI_ADD_10	194 —	B0_ADD_11	210 -	BO_ADD_11	226 -	B0_ADD_11	
338 -	BI_ADD_11		354	BI_ADD_11	195 —	BO_ADD_12	211 -	BO_ADD_12	227 -	BO_ADD_12	
339 -	BI_ADD_12		365 -	BI_ADD_12	196 —	BO_ADD_13	212 -	BO_ADD_13	228 -	B0_ADD_13	
340 -	BI_ADD_13		356 -	BI_ADD_13	197 —	BO_ADD_14	213 -	BO_ADD_14	229 -	BO_ADD_14	
341 -	BI_ADD_14		357 -	BI_ADD_14	198 —	80_ADD_15	214-	BO_ADD_15	230 -	B0_ADD_15	
342 -	BI_ADD_15		358 -	BI_ADD_15	199 —	B0_ADD_16	215 -	80_ADD_16	231 -	B0_ADD_16	
343 -	BI_ADD_16	_	359 -	BI_ADD_16	1	19_80	I	19_90	I	1 19 80	
	F 18 81			18_81							

Figure 6-36. Example of 1794-IT8 Read and Write GAP Blocks

To read the analog input words for the 1794-IT8 module, individual FB\_AI blocks were used. Again, the addressing for the analog input blocks need to be in bytes. To convert from spreadsheet bit addresses to bytes, take the first bit of the word in the spreadsheet for the 1794-IT8 module and divide by 8 bits/byte (208÷8=26). Repeat this calculation for the rest of the addresses for each channel. In order to read the output from the 1794-IT8 module correctly, the FB\_AI block must be scaled appropriately. According to the 1794-IT8 manual, the AI\_RL\_1 (Minimum Temp) and AI\_RH\_1 (Maximum Temp) must be scaled to ten times the AI\_BL\_1 (Scale Low) and AI\_BH\_1 (Scale High) values. Do not use the –95 to 2502 °F range indicated in Figure 6-37 1794-IT8 Write Word 1 and 2, above, because it is in error. Use Figure 6-37 1794-IT8 Input Scaling, below, for type K thermocouple range of –454 to 2502 °F.

Manual 85586V2

Input Type	Range	Scaling	Maximum Resolution
Millivolt	-76.50 to +76.50mV	-7650 to +7650	10µV
Type B	300 to 1800°C	3000 to 18000	0.1°C
Type E	-270 to 1000°C	2700 to 10000	0.1ºC
Type J	-210 to 1200°C	-2100 to 12000	0.1°C
Туре К	-270 to 1372°C	-2700 to 13720	0.1°C
Type R	-50 to 1768°C	-500 to 17680	0.1°C
Type S	-50 to 1768°C	-500 to 17680	0.1ºC
Туре Т	-270 to 400°C	-2700 to 4000	0.1ºC
Type N	-270 to 1300°C	-2700 to 13000	0.1°C
Type C	0 to 2315°C	0 to 23150	0.1°C
Type B	572 to 3272°F	5720 to 32720	0.1ºF
Type E	-454 to 1832°F	-4540 to 18320	0.1ºF
Type J	-346 to 2192°F	-3460 to 21920	0.1°F
Туре К	-454 to 2502°F	-4540 to 25020	0.1°F
Type R	-58 to 3214°F	-580 to 32140	0.1ºF
Type S	-58 to 3214°F	-580 to 32140	0.1ºF
Туре Т	-454 to 752°F	-4540 to 7520	0.1ºF
Type N	-450 to 2372°F	-4500 to 23720	0.1ºF
Туре С	32 to 4199°F	320 to 41990	0.1ºF

# Input Scaling

Note: In thermocouple mode, scaled number has an implied decimal point 1 digit from the right. For example, if reading is 18000, temperature is 1800.0. In millivolt mode, the implied decimal point is to the left of the last 2 digits. For example, if reading is 2250, actual reading is 22.50mV

Figure 6-37. 1794-IT8 Input Scaling

Again, from the 1794-IT8 manual, the range of the cold junction (reference junction) sensor is 0-70 °C. This converts to 32 to 158 °F. It has been found that the AI\_RL\_1 and AI\_RH\_1 must be scaled to one hundred times the AI\_BL\_1 and AI\_BH\_1 values. See Figure 6-38 for example of 1794-IT8 GAP Analog Read Blocks.



Figure 6-38. Example of 1794-IT8 GAP Analog Read Blocks

### Allen-Bradley RTD Input (1794-IR8) Module



See Figure 6-39 for example of 1794-IR8 module wiring.



Figure 6-39. Example of 1794-IR8 Module Wiring

The memory map indicates that there are eleven read addresses and 3 write address. The condensed format used to set up the address spreadsheet specifies eleven read addresses and 3 write addresses also. See Figure 6-40 for the input memory map and Figures 6-41 through 6-44 for the output memory map for the 1794-IR8 module.

RTD Anal	alog Input Module (1794-IR8) Read Words															
Decimal Bit	15	14	13	12	11	10	09	80	07	06	05	04	03	02	01	00
Octal Bit	17	16	15	14	13	12	11	10	07	06	05	04	03	02	01	00
Word 0		Reserved														
1							С	hannel 0 I	nput Da	nta						
2							С	hannel 1 I	nput Da	ata						
3		Channel 2 Input Data														
4		Channel 3 Input Data														
5							С	hannel 4 I	nput Da	ata						
6							С	hannel 5 I	nput Da	ata						
7							С	hannel 6 I	nput Da	ata						
8							С	hannel 7 I	nput Da	ata						
9		Overrange Bits Underrange Bits														
10	0	0 0 0 Bad Cal Cal Cal 0 Diagnostic Pwr Reserved 0 0 Cal Done Range Status Bits Up Reserved 0 0							0							

Figure 6-40. 1794-IR8 Module Input Memory Map

Underrange bits—These bits are set if the input signal is below the input channel's minimum range.

Overrange bits—These bits are set if 1), the input signal is above the input channel's maximum range, or 2), an open detector is detected.

Powerup bit—This bit is set (1) until configuration data is received by the module.

Critical Error bits—If these bits are anything other than all zeroes, return the module to the factory for repair.

Calibration Range bit—Set to 1 if a reference signal is out of range during calibration

Calibration Done bit—Set to 1 after an initiated calibration cycle is complete. Calibration Bad bit—Set to 1 if the channel has not had a valid calibration.

Decimal Bit	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Octal Bit	17	16	15	14	13	12	11	10	07	06	05	04	03	02	01	00
Word 0	8-bit Calibration Mask								Cal Clk	Cal Hi Cal Lo	Filter Cutoff E			Enh	M	DT
1		RTD 3	Туре			RTD	2 Туре			RTD 1 T	уре			RTD 0 T	уре	
2		RTD 7 Type RTD 6 Type								RTD 5 T	уре			RTD 4 T	уре	
Where: Enh = Enhanced																

RTD Analog Input Module (1794-IR8) Write Words

IDT = Module Data Type

Figure 6-41. 1794-IR8 Module Output Memory Map

# AtlasPC Digital Control, Vol. II (Distributed I/O)

Word	Dec. Bits (Octal Bits)		Description									
Write word 0	00-01	Modul	odule Data Type									
		Bit	01 00									
			0	0	°C (default)							
			0	1	oF							
			1	0	Bipolar counts scaled between -32768 and +32767							
			1	1	1 Unipolar counts scaled between 0 and 65535							
	02	Enhan compa reduce	anced mode select – measures voltage drop across a precision resistor in the module to pare with the unknown input. This improves module temperature drift characteristics, but ces module throughput.									
	03-05	A/D Fi	Filter First Notch Frequency									
		Bit	it 05 04 03 Definition									
			0	0 0 10Hz (default)								
			0	0	1	25Hz						
			0	1	0	50Hz						
			0	1	1	60Hz						
			1	0	0	100Hz						
			1	0	1	250Hz						
			1	1	0	500Hz						
			1	1000Hz								
	06	Calibra	s bit is set during gain calibration; reset during offset calibration.									
	07	Calibra initiate	ation clo calibrati	o <b>ck</b> – thi on.	s bit mus	st be set to 1 to prepare for a calibration cycle; then reset to 0 to						
	08-15 (10-17)	Calibra Bit 8 co	ation ma	lsk – Th ds to ch	e chann annel 0,	el, or channels, to be calibrated will have the correct mask bit set. bit 9 to channel 1, and so on.						

Figure 6-42. 1794-IR8 Write Word 0

#### Hardware First Notch Filter

A/D Filter First Notch Frequency (effective resolution)	10Hz (16-bits)	25Hz (16-bits)	50Hz (16-bits)	60Hz (16-bits)	100Hz (16-bits)	250Hz (13-bits)	500Hz (11-bits)	1000Hz (9-bits)
Number of channels scanned			Sys	tem Throughp	out (in ms an	d s)		
1	325	145	85	75	55	37	31	28
2	650	290	170	150	110	74	62	56
3	975	435	255	225	165	111	93	84
4	1.3s	580	340	300	220	148	124	112
5	1.625s	725	425	375	275	185	155	140
6	1.95s	870	510	450	330	222	186	168
7	2.275s	1.015s	595	525	385	259	217	196
8	2.60s <sup>1</sup>	1.16s	680	600	440	296	248	224
1 Default setting		-		-				

Figure 6-43. 1794-IT8 Hardware First Notch Filter

Word	Dec. Bits (Octal Bits)		Description						
Write Word 1	00-03	Chann	hannel 0 RTD Type						
		Bit	03	02	01	00	RTD Type – Range		
			0	0	0	0	Resistance (default)		
			0	0	0	1	No sensor connected – do not scan		
			0	0	1	0	100 ohm Pt $\alpha$ = 0.00385 Euro (–200 to +870°C)		
			0	0	1	1	100 ohm Pt $\alpha$ = 0.003916 U.S. (–200 to +630°C)		
			0	1	0	0	200 ohm Pt $\alpha$ = 0.00385 Euro (–200 to +630°C)		
	0         1         0         1         500 ohm Pt α = 0.00385 Euro (           0         1         1         0         Reserved						500 ohm Pt $\alpha$ = 0.00385 Euro (–200 to +630°C)		
							Reserved		
			0	1	1	1	10 ohm Copper (-200 to +260°C)		
			1	0	0	0	120 ohm Nickel (-60 to +250°C)		
			1	0	0	1	100 ohm Nickel (-60 to +250°C)		
			1 0 1 0 200 ohm Nickel (-60 to			1	200 ohm Nickel (-60 to +250°C)		
			1	0	1	1	500 ohm Nickel (-60 to +250°C)		
			1	1	0	0	Reserved		
			1101 to	o 1111 -	Reserve	ed			
	04-07	Chann	el 1 RTD	) Type (s	see bits	00-03)			
	08-11	Chann	el 2 RTD	) Type (s	see bits	00-03)			
Write Word 2	00-03	Chann	el 4 RTD	) Type (s	ee write	word 1,	bits 00-03)		
	04-07	Chann	el 5 RTD	) Type (s	see write	word 1,	bits 00-03)		
	08-11	Chann	el 6 RTD	) Type (s	ee write	word 1,	bits 00-03)		
	12-15	Chann	el 7 RTD	) Type (s	ee write	word 1,	bits 00-03)		

Figure 6-44. 1794-IT8 Write Word 1 and 2

In this example, the first read block is set up to monitor the all of the under and overrange bits on the module. The second read block monitors the Powerup bit, Critical Error bits, Calibration Range bit, Calibration Done bit, and Calibration Bad bit. The first write word(1) sets the module for °F units, 100 Hz filtering, and no calibration. The second write word(2) sets the module for 100 ohm Pt Euro RTD on channels 0, 1, 2, and 3. The third write word(3) sets the module for 100 ohm Pt Euro RTD for channels 4, 5, 6, and 7. See Figure 6-45 for GAP read and write block example.

### AtlasPC Digital Control, Vol. II (Distributed I/O)

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G1N7_IR8	G1N7_IR8 PEAR2	G1N7_IR8	G1N7_IR8 W/PITE2	G1N7_IR8
(A1/6/G1/N7/RTD)-IO_CHANNEL	(A1/6/G1/N7/RTD)-10_CHANNEL	*TRUE-B0_V_1	*FALSE-B0_V_1	*FALSE-B0_V_1
CHANNEL 1 UNDERRANGE BI_C_1	NOT USED -BI_C_1	*FALSE-B0_V_2	*TRUE-B0_V_2	-( <u>A1/6/G1/N7/RTD</u> ) I0_CHANNEL-( <u>A1/6/G1/N7/RTD</u> ) *TRUE-B0_V_2
CHANNEL 2 UNDERRANGE -BI_C_2	NOT USED -BI_C_2	*FALSE-B0_V_3	*FALSE-B0_V_3	*FALSE-BO_V_3
CHANNEL3 UNDERRANGE BI_C_3	NOT USED BI_C_3	*FALSE-B0_V_4	*FALSE-B0_V_4	*FALSE-B0_V_4
CHANNEL 4 UNDERRANGE - BI_C_4	POWER UP BIT-BI_C_4	*FALSE-B0_V_5	*FALSE-B0_V_5	*FALSE-B0_V_5
CHANNEL 5 UNDERRANGE BI_C_5	CRITICAL ERROR BITS - BI_C_5	*TRUE-80_V_6	*TRUE-B0_V_6	*TRUE-80_V_6
CHANNEL6 UNDERRANGE BI_C_6	CRITICAL ERROR BIT-BI_C_6	*FALSE-00_V_7	*FALSE-B0_V_7	"FALSE-B0_V_7
CHANNEL7 UNDERRANGE-BI_C_7	CRITICAL ERROR BIT BI_C_7	*FALSE-B0_V_8	*FALSE-B0_V_8	*FALSE-B0_V_8
CHANNEL® UNDERRANGE BI_C_8	NOT USED -BI_C_8	*FALSE-BO_V_9	*FALSE-B0_V_9	*FALSE-BO_V_9
CHANNEL 1 OVERRANGE BI_C_9	CALIBRATION OUT OF RANGE-BI_C_9	*FALSE-80_V_10	*TRUE-B0_V_10	*TRUE-80_V_10
CHANNEL 2 OVERRANGE BI_C_10	CALIBRATION DONE-BI_C_10	*FALSE-00_V_11	*FALSE-B0_V_11	*FALSE-80_V_11
CHANNEL3 OVERRANGE BI_C_11	CALIBRATION BAD -BI_C_11	*FALSE-0_V_12	*FALSE-B0_V_12	*FALSE-80_V_12
CHANNEL 4 OVERRANGE BI_C_12	NOT USED BI_C_12	*FALSE-80_V_13	*FALSE-B0_V_13	"FALSE-B0_V_13
CHANNEL 5 OVERRANGE BI_C_13	NOT USED -BI_C_13	*FALSE-00_V_14	*TRUE-80_V_14	*TRUE-80_V_14
CHANNEL® OVERRANGE BI_C_14	NOT USED -BI_C_14	*FALSE-80_V_16	*FALSE-B0_V_15	*FALSE-80_V_15
CHANNEL 7 OVERRANGE BI_C_16	NOT USED BI_C_15	*FALSE-80_V_16	*FALSE-B0_V_16	"FALSE-80_V_16
CHANNELS OVERRANGE BI_C_16	NOT USED -BI_C_16	264-80_ADD_1	280 - 80_ADD_1	296-B0_ADD_1
520 - BI_ADD_1	536 - BI_ADD_1	265-00_ADD_2	281-B0_ADD_2	297-80_ADD_2
521 - BI_ADD_2	537 - BI_ADD_2	266 - 80_ADD_3	282 - BO_ADD_3	298-B0_ADD_3
522 - BI_ADD_3	538 - BI_ADD_3	267-80_ADD_4	283 - B0_ADD_4	299-80_ADD_4
523 - BI_ADD_4	539 - BI_ADD_4	268-00_ADD_5	284-80_ADD_5	300-B0_ADD_5
624 - BI_ADD_6	540 - BI_ADD_5	269 - 80_ADD_6	285 - BO_ADD_6	301-B0_ADD_6
525 - BI_ADD_6	541 - BI_ADD_6	270-80_ADD_7	286 - B0_ADD_7	302-B0_ADD_7
526 - BI_ADD_7	542 - BI_ADD_7	271-80_ADD_8	287 - 80_ADD_8	303-80_ADD_8
627 - BI_ADD_8	543 - BI_ADD_8	256 - 80_ADD_9	272 - 80_ADD_9	288-B0_ADD_9
512 BI_ADD_9	528 - BI_ADD_9	257-80_ADD_10	273 - BO_ADD_10	289-B0_ADD_10
513 - BI_ADD_10	529 - BI_ADD_10	258-80_ADD_11	274-B0_ADD_11	290-B0_ADD_11
514-BI_ADD_11	530 - BI_ADD_11	259-80_ADD_12	275-B0_ADD_12	291-B0_ADD_12
515 BI_ADD_12	531-BI_ADD_12	260-80_ADD_13	276 - B0_ADD_13	292-B0_ADD_13
516 - BI_ADD_13	632 - BI_ADD_13	261-80_ADD_14	277 - 80_ADD_14	293-B0_ADD_14
517 - BI_ADD_14	533 - BI_ADD_14	262-00_ADD_15	278-80_ADD_15	294-B0_ADD_15
518 - BI_ADD_15	534-BI_ADD_15	263 - 80_ADD_16	279 - 80_ADD_16	295-B0_ADD_16
519 BI_ADD_16 FB_BI	535 - BI_ADD_16 F8_BI	F8_80	F8_80	<u> </u>

Figure 6-45. Example of 1794-IR8 Read and Write GAP Blocks

To read the analog input words for the 1794-IR8 module, individual FB\_AI blocks were used. Again, the addressing for the analog input blocks needs to be in bytes. In order to read the output from the 1794-IR8 module correctly, the FB\_AI block must be scaled appropriately. According to the 1794-IR8 manual, the AI\_RL\_1 (Minimum Temp) and AI\_RH\_1 (Maximum Temp) must be scaled to ten times the AI\_BL\_1 (Scale Low) and AI\_BH\_1 (Scale High) values. From the 1794-IR8 Input Scaling, it can be seen that the 100 ohm Pt Euro RTD range is – 328 to 1598 °F. See Figure 6-46 for Input scaling for RTDs.

Input	Scali	ng
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Range	Degrees	Counts	Maximum Resolution
100 ohm Pt Euro	-328 to +1598°F	-3280 to +15980	0.1ºF
100 ohm Pt U.S	-328 to +1166°F	-3280 to +11660	0.1ºF
200 ohm Pt Euro	-328 to +1166°F	-3280 to +11660	0.1ºF
500 ohm Pt Euro	-328 to +1166°F	-3280 to +11660	0.1ºF
100 ohm Nickel	-76 to +482°F	-760 to +4820	0.1ºF
120 ohm Nickel	-112 to +500°F	-1120 to +5000	0.1°F
200 ohm Nickel	-76 to +482°F	-760 to +4820	0.1°F
500 ohm Nickel	-76 to +482°F	-760 to +4820	0.1ºF
10 ohm Copper	-328 to +500°F	-3280 to +5000	0.1°F

Note: Temperature data has an implied decimal point 1 space to the right of the last digit. (divide by 10). For example, a readout of 1779° would actually be 177.9°.

Figure 6-46.1794-IR8 Input Scaling

#### See Figure 6-47 for example of 1794-IR8 GAP Analog Read Blocks.



Figure 6-47. Example of 1794-IR8 GAP Analog Read Blocks

# Allen-Bradley Flex I/O Modbus Configuration

MODBUS is an application layer messaging protocol, at level 7, as defined in the OSI (Open System Interconnection) model. It provides client/server communication between devices connected on different types of buses or networks. It is a request/reply protocol and offers services specified by function codes. MODBUS function codes are elements of MODBUS request/reply PDUs (Protocol Data Unit).

Modicon developed the Modbus addressing scheme around the data table and I/O structure in Modicon PLCs. Allen-Bradley Flex I/O is a modular system which combines the functions of terminal blocks and I/O modules for distributed I/O. Each Flex I/O system has the following components: a Base Controller and one or more I/O Module(s). Flex I/O systems can contain up to 8 I/O modules per slave (node). An external +24 Vdc power supply is required.

In this example, one 3170-MBS MODBUS adapter from ProSoft Technology, Inc. is interfaced with seven terminal base units with installed FLEX I/O modules, forming a FLEX I/O system.

The 3170-MBS is a Network Interface Adapter that communicates between the FLEX I/O module backplane and AtlasPC/Master across a serial RS-485 connection. The 3170-MBS module is a slave device to the AtlasPC control, and is a master controller of the FLEX I/O modules. The I/O data exchange occurs as follows: Output data is sent from the AtlasPC control across the RS-485 connection to the 3170-MBS adapter. The network interface adapter then automatically transfers the data across the FLEX I/O backplane to the output modules. Inputs from the input modules are collected by the network interface adapter via the backplane and sent across the RS-485 connection to the AtlasPC control.

The most common data space used is the 4xxxx space using the Function Codes 3, 6 and 16. This space is used to transfer 16 bit register values and can be used to transfer bit mapped data. In this example of the Allen-Bradley configuration, only the 4xxxx address space is used, which results in all discrete communications being done in analog words.

Each Flex module has 60 words of address space (30 Input or Read addresses and 30 Output or Write addresses). Data can be mapped in two directions, horizontal or vertical. There are 15 Horizontal and 15 Vertical addresses assigned per module. With horizontal addressing, the adapter addresses the first input and output word for each module incrementally across the modules. 40001 for module 0, 40002 for module 1 and so on. Vertical addressing increments all the words for each module. For example, the vertical read words for slot 0 start with 41001 and increment to 41015.

In order to simplify the nomenclature used in creating the GAP application, certain naming conventions were changed with respect to the manufacturer's naming convention. In this example, Woodward refers to the node address as the Group address. The 3170-MBS Group address (Node address), is set by a dip switch located on the 3170-MBS module. In this example the address is set to 01.

Upon power–up, the 3170-PDP goes to an initialization state and performs a self–test (memory check, data memory clear. If a failure occurs, the interface adapter transitions to a faulted state and waits for reset (cycle power). Otherwise, the adapter begins monitoring the network (run state) for messages.

In this example, the power wiring is daisy–chained to the Network Interface adapter and then to the terminal bases. See Figure 6-48 for Allen-Bradley Flex I/O configuration layout.



Figure 6-48. Allen-Bradley Flex I/O Configuration

### Address Spreadsheet

The I/O map for a module is divided into read words and write words. Read words consist of input and status words, and write words consist of output and configuration words. The number of read words or write words can be 0 or more.

To keep track of the addressing for all of the reads and writes, the creation of an address spreadsheet is very useful. This address spreadsheet can be derived from the network interface module (head) 3170-MBS User Manual. The Allen-Bradley I/O modules can be addressed in two ways (Horizontal or Vertical). It has been found that vertical addressing works best with the sequential nature of the MODBUS\_M GAP block repeat field functionality. See Table 12.7.1.3-1 for address spread sheet for this example.

Vertical	Read Add	resses					
IB16	OV16	OW8	IE8/B	OE4/B	IT8	IR8	Empty Slot
41001	41016	41031	41046	41061	41076	41091	41106
41002	41017	41032	41047	41062	41077	41092	41107
41003	41018	41033	41048	41063	41078	41093	41108
41004	41019	41034	41049	41064	41079	41094	41109
41005	41020	41035	41050	41065	41080	41095	41110
41006	41021	41036	41051	41066	41081	41096	41111
41007	41022	41037	41052	41067	41082	41097	41112
41008	41023	41038	41053	41068	41083	41098	41113
41009	41024	41039	41054	41069	41084	41099	41114
41010	41025	41040	41055	41070	41085	41100	41115
41011	41026	41041	41056	41071	41086	41101	41116
41012	41027	41042	41057	41072	41087	41102	41117
41013	41028	41043	41058	41073	41088	41103	41118
41014	41029	41044	41059	41074	41089	41104	41119
41015	41030	41045	41060	41075	41090	41105	41120
Vertical	Write Add	Iresses					
IB16	OV16	OW8	IE8/B	OE4/B	IT8	IR8	Empty Slot
41201	41216	41231	41246	41261	41276	41291	41306
41202	41217	41232	41247	41262	41277	41292	41307
41203	41218	41233	41248	41263	41278	41293	41308
41204	41219	41234	41249	41264	41279	41294	41309
41205	41220	41235	41250	41265	41280	41295	41310
41206	41221	41236	41251	41266	41281	41296	41311
41207	41222	41237	41252	41267	41282	41297	41312
41208	41223	41238	41253	41268	41283	41298	41313
41209	41224	41239	41254	41269	41284	41299	41314
41210	41225	41240	41255	41270	41285	41300	41315
41211	41226	41241	41256	41271	41286	41301	41316
41212	41227	41242	41257	41272	41287	41302	41317
41213	41228	41243	41258	41273	41288	41303	41318
41214	41229	41244	41259	41274	41289	41304	41319
41015	41230	41245	41260	41275	41290	41305	41320

Table 6-4. Modbus Word Address Spreadsheet

In order to assign a specific function to each address, review each module's memory map. These memory maps define which addresses are used within the Address Spreadsheet. Not all of the 15 vertical addresses assigned to each module are used. Only the number of addresses specified in the memory map for each module are used. The remaining addresses are undefined. Those addresses defined in the individual I/O module's memory maps are highlighted in Table 12.7.1.3-1 above.

Use the following documents from the manufacturer to obtain the Memory Maps and related information.

Module	Document P/N
Discrete Input (Sink)	1794-5.4
Discrete Output (Sink)	1794-5.29
Discrete Output (Relay)	1794-5.19
Analog Input (Current)	1794-5.6
Analog Output (Current)	1794-5.5
Thermocouple Input	1794-6.5.7
RTD Input	1794-6.5.4
Modbus Interface	3170-MBS USER MANUAL

### Nomenclature

When creating a new GAP application, it is important to establish a well organized block naming convention up front. Once done, it is easier to find specific functions and I/O within a large GAP application. Though not shown in this example, the Category and Block Names could follow similar nomenclature rules to those shown in Chapter 1 (Profibus).

#### **GAP** Application

In order to communicate between the Atlas serial RS-485 port and the 3170-MBS, a MOD\_PORT and MODBUS\_M block must be defined in GAP. The MOD\_PORT block defines the serial communications baud rate, stop, parity, and type of interface (RS-232, 422, 485). The MODBUS\_M block defines the addressing for Modbus communications between the Atlas and the distributed I/O. Based on the Address Spreadsheet, this block can be customized to read and write to appropriate addresses. See Figure 6-49 for MODBUS\_M/MOD\_PORT setup example.



Figure 6-49. MODBUS\_M Block Example

The E\_ERR\_1\_x output field on the MODBUS\_M block is used to display Exception Error on PORT\_1 per RPTx. It latches TRUE when an exception error is detected. E\_NUM\_1\_X (hidden) displays the error number. See Table 12.7.1.3-3 for exception errors.

CODE	NAME	MEANING							
The fo	The following are generated by the slave.								
00	NO ERROR	Error free							
01	ILLEGAL FUNCTION	Message function received is not an allowable action for addressed slave. (Unsupported or illegal function code).							
02	ILLEGAL DATA ADDRESS	Address referenced in data field is not an allowable address for the addressed slave location. (Master requested data which is not configured from slave).							
03	ILLEGAL DATA VALUEA	mount of data requested from slave was too large for slave to return in a single response.							
The fo	llowing are generat	ed by the master.							
09	CHECKSUM ERROR	Error in checksum in message from slave. Can indicate link quality and/or noise problems.							
10	GARBLED MESSAGE	Data received from the slave, but is too short to be a valid Modbus message/response.							
20	UNSOLICITED RESPONSE	Unsolicited message received from slave.							
21	BAD FC IN RESPONSE	Slave returned a message with a different function code from the command sent.							
22	BAD ADD IN RESPONSE	Slave returned a message with a different address from the command sent.							
23	NO SLAVE RESPONSE	No response from slave.							
24	MOE/CODER ERROR	MOE/CODER error.							
25	INTERNAL SYS ERROR	Internal system error.							

Table 6-5. MODBUS\_M Exception Errors

The L\_ERR\_1\_x is used to display Link Error on PORT\_1 for RPTx. It goes TRUE when the slave fails to answer a data request. If a response isn't received in TIME\_OUT\_x seconds, the request is retried. If a response isn't received in TIME\_OUT\_x seconds after the request is retried, then this output is set true.

While waiting for a response from one slave, the master is not communicating with the other slaves. So, if multiple slaves fail at the same time (i.e. broken cable), the L\_ERR\_1\_x for the first slave attempted will occur at 2 x TIME\_OUT\_x. But, the second L\_ERR\_1\_x won't go true until 2 x TIME\_OUT\_x after the first failure because no communications are attempted with that slave until after the first has timed out.

The 3170-MBS RS-485 communications setup must be configured manually with two DIP switches located on the Adapter. These DIP switches must reflect the settings specified in the MOD\_PORT and MODBUS\_M blocks. The MOD\_PORT block defaults to 8 data bits per word. These setting were set as follows for this example:

Baud Rate	38400
Stop Bit	1
Parity	Off
Data Bits	8
Modbus Mode	RTU
Address	001

In order to limit the size of the MODBUS\_M address repeat groups, four repeat groups were set up. These groups consisted of:

Group 1 addresses 40121-40173 (Adapter Status Words) Group 2 addresses 41001-41120 (Analog Read), 41201-41245 (Analog Write) Group 3 addresses 41246-41290 (Analog Write) Group 4 addresses 41291-41294 (Analog Write)

The analog writes were split into small groups with no more than 45 analog write addresses each. It was found that the Allen-Bradley adapter couldn't accept more than 45 write requests per group. If more than 45 analog write addresses are listed, the 3170-MBS will not communicate with the AtlasPC control. From the Address Spreadsheet, it can be seen that the Allen-Bradley modules require all read and write addresses be in the 40000 block of addresses. The AR\_F\_CODE field specifies the Analog Read Function Code for Modbus. By setting the AR\_F\_CODE field to 3, the MODBUS\_M block will access addresses 40001-4FFFF for reads. Address offsets are specified in the AR\_ADD\_X fields in order to limit the number of repeats within each address group. See Figure 6-50 for example of MODBUS\_M repeat fields.

Group 1			Group 2			Group 3			Group 4	
hide < S ADD 1	▲ <b>1</b>	hide	< S_ADD_2	1	hide	< S_ADD_3	1	hide	< S_ADD_4	1
hide < S IP 1 1		hide	< S_IP_1_2	(0)	hide	< S_IP_1_3	(0)	hide	< S_IP_1_4	(0)
hide < S IP 2 1		hide	< S_IP_2_2	(0)	hide	< S_IP_2_3	(0)	hide	< S_IP_2_4	(0)
hide < S IP 3 1	lm	hide	< S_IP_3_2	(0)	hide	< S_IP_3_3	(0)	hide	< S_IP_3_4	(0)
hide < S IP 4 1		hide	< S_IP_4_2	(0)	hide	< S_IP_4_3	(0)	hide	< S_IP_4_4	(0)
hide < S PORT 1		hide	< S_PORT_2	(0)	hide	< S_PORT_3	(0)	hide	< S_PORT_4	(0)
show < I MOD 1	*FALSE	show	< I_MOD_2	*FALSE	show	< I_MOD_3	*FALSE	show	<i_mod_4< td=""><td>*FALSE</td></i_mod_4<>	*FALSE
show < E RST 1		show	< E_RST_2	*FALSE	show	< E_RST_3	*FALSE	show	< E_RST_4	*FALSE
hide < TIMEOUT 1	[1.5]	hide	< TIMEOUT_2	(1.5)	hide	< TIMEOUT_3	(1.5)	hide	< TIMEOUT_4	(1.5)
hide > E NUM 1 1		hide	> E_NUM_1_2		hide	> E_NUM_1_3		hide	> E_NUM_1_4	
show > E ERR 1 1		show	> E_ERR_1_2		show	> E_ERR_1_3		show	> E_ERR_1_4	
show > L ERR 1 1		show	> L_ERR_1_2		show	> L_ERR_1_3		show	> L_ERR_1_4	
hide > E NUM 2 1		hide	> E_NUM_2_2		hide	> E_NUM_2_3		hide	> E_NUM_2_4	
show > E ERR 2 1		show	> E_ERR_2_2		show	> E_ERR_2_3		show	> E_ERR_2_4	
show > L ERR 2 1		show	> L_ERR_2_2		show	> L_ERR_2_3		show	> L_ERR_2_4	
hide < BW_ADD_1		hide	< BW_ADD_2		hide	< BW_ADD_3		hide	< BW_ADD_4	
>> RPTbw1		>>	RPTbw2		>>	RPTbw3		>>	RPTbw4	
hide < BR F CODE	[2]	hide	< BR_F_CODE_	(2)	hide	< BR_F_CODE_	(2)	hide	< BR_F_CODE_	(2)
hide < BR_ADD_1		hide	< BR_ADD_2		hide	< BR_ADD_3		hide	< BR_ADD_4	
>> RPTbr1		>>	RPTbr2		>>	RPTbr3		>>	RPTbr4	
hide < AR F CODE	3	hide	< AR_F_CODE_:	3	hide	< AR_F_CODE_:	3	hide	< AR_F_CODE_	3
hide < AR_ADD_1	120	hide	< AR_ADD_2	1000	hide	< AR_ADD_3		hide	< AR_ADD_4	
>> RPTar1		>>	RPTar2		>>	RPTar3		>>	RPTar4	
hide < AW_ADD_1		hide	< AW_ADD_2	1200	hide	< AW_ADD_3	1245	hide	< AW_ADD_4	1290
>> RPTaw1		>>	RPTaw2		>>	RPTaw3		>>	RPTaw4 👻	

Figure 6-50. MODBUS\_M Block RPT Window Example

Within the MODBUS M RPT window, there are four repeats for each group (RPTbw1, RPTbr1, RPTar1, and RPTaw1). Each one of these RPT fields opens another window which displays the addresses assigned for that particular group. See specific module sections below for memory map function assignment. Example for Module 1 status bits (AR\_V\_1\_1): since group one uses AR F CODE = 3, the starting address is 40000. The AR ADD 1 offset is 120. Therefore the Module 1 status word (AR V 1 1) has an address of 40000 + 120 + 1 = 40121. All of the addresses specified in the Address Spreadsheet are mapped into MODBUS M block by applying this formula. See Figures 6-51, 6-52, 6-53, 6-54, and 6-55 for Groups 1, 2, 3, and 4 read/write address windows. Only those addresses specified in the Memory map/Address Spreadsheet are shown to abbreviate the figures. Group 1 doesn't contain any RPTbw1, RPTbr1, or RPTaw1 repeat fields because it is used for the Adapter Status Words. See Prosoft Modbus Interface (3170-MBS) Module section below for memory map functionality. Figure 6-51 shows the read addresses for Group 1 (40121-40173, Adapter Status Words).

	hide	< AR_C_1_1	-	MODULE FAULTS & LAST STATE BITS	 hide < AR_C_1_34	MBS REVISION LEVEL
	hide	> AR_V_1_1			hide > AR_V_1_34	
	hide	< AR M 1 1		(1.0)	hide < AR_M_1_34	(1.0)
	hide	< AR D 1 1		(0.0)	hide < AR_D_1_34	(0.0)
l	hide	ARC12		MODULE 1 STATUS BITS	hide < AR_C_1_35	MBS BATCH NUMBER
	hide	> AR V 1 2			hide > AR_V_1_35	
	hide	(AR M 1 2		(1.0)	hide < AR_M_1_35	(1.0)
l	hide	ABD12		0.0	hide < AR_D_1_35	(0.0)
	hide	KAR C 1 3		MODULE 2 STATUS BITS	hide < AR_C_1_36	FUNCTION CODE 1 COUNTER
	hide	> AR V 1 3			hide > AR_V_1_36	
	hide	KAR M 1 3		(1.0)	hide < AR_M_1_36	(1.0)
	hide	KAR D 1 3		io.oi	hide < AR_D_1_36	(0.0)
	hide	KAR C 1 4		MODULE 3 STATUS BITS	hide < AR_C_1_37	FUNCTION CODE 2 COUNTER
	hide	> AB V 1 4			hide > AR_V_1_37	
	hide	KAR M 1 4		(1.0)	hide < AR_M_1_37	(1.0)
l	hide	ABD14		(n.m	hide < AR_D_1_37	(0.0)
	hide	ABC15		MODULE 4 STATUS BITS	hide < AR_C_1_38	FUNCTION CODE 3 COUNTER
	hide	ARV15			hide > AR_V_1_38	
	hide	< AR M 1 5		(1.0)	hide < AR_M_1_38	(1.0)
	hide	ARD 15		(0.0)	hide < AR_D_1_38	(0.0)
	hide	ARC16		MODULE 5 STATUS BITS	hide < AR_C_1_39	FUNCTION CODE 4 COUNTER
	hide	ABV16			hide > AR_V_1_39	
	hide	< AR M 1 6		(1.0)	hide < AR_M_1_39	(1.0)
	hide	ARD 16		(0.0)	hide < AR_D_1_39	(0.0)
	hide	< AR C 1 7		MODULE 6 STATUS BITS	hide < AR_C_1_40	FUNCTION CODE 5 COUNTER
	hide	> AR V 1 7			hide > AR_V_1_40	
	hide	< AR M 1 7		(1.0)	hide < AR_M_1_40	(1.0)
	hide	< AR D 1 7		(0.0)	hide < AR_D_1_40	(0.0)
	hide	ARC18		MODULE 7 STATUS BITS	hide < AR_C_1_41	FUNCTION CODE 6 COUNTER
	hide	> AR V 1 8			hide > AR_V_1_41	
	hide	< AR_M_1_8		(1.0)	hide < AR_M_1_41	(1.0)
	hide	< AR_D_1_8		(0.0)	hide < AR_D_1_41	(0.0)
	hide	< AR_C_1_9		MODULE 8 STATUS BITS	hide < AR_C_1_42	FUNCTION CODE 15 COUNTER
	hide	> AR_V_1_9			hide > AR_V_1_42	
1	hide	< AR_M_1_9		(1.0)	hide < AR_M_1_42	(1.0)
I	hide	< AR_D_1_9		(0.0)	hide < AR_D_1_42	(0.0)
ĺ					hide < AR_C_1_43	FUNCTION CODE 16 COUNTER
					hide > AR_V_1_43	
					hide < AR_M_1_43	(1.0)
					111 1 40 0 1 42	100.00

ide	< AR_C_1_51	RESPONSES TO HOST
ide	> AR_V_1_51	
ide	< AR_M_1_51	(1.0)
ide	< AR_D_1_51	(0.0)
ide	< AR_C_1_52	NO RESPONSES TO HOST
ide	> AR_V_1_52	
ide	< AR_M_1_52	(1.0)
ide	< AR_D_1_52	(0.0)
ide	< AR_C_1_53	LAST DETECTED ERROR
ide	> AR_V_1_53	
ide	< AR_M_1_53	(1.0)
ide	< AR D 1 53 🖵	(0.0)

Figure 6-51. MODBUS\_M Block Group 1 Analog Read RPT Example

Figure 6-52 shows all of the used read addresses for Group 2 (41001-41120, Analog Read)

I	hide	< AR_C_2_1 🔺	IB16 CHANNELS	hide < AR_C_2_61	0E4/B OPEN WIRE & POWER UP BITS	hide	< AR_C_2_97	IR8 CH6
I	hide	> AR_V_2_1		hide > AR_V_2_61		hide	> AR_V_2_97	
I	hide	< AR M 2 1	(1.0)	hide < AR_M_2_61	(1.0)	hide	< AR_M_2_97	(1.0)
I	hide	< AR D 2 1	(0.0)	hide < AR_D_2_61	(0.0)	hide	< AR_D_2_97	(0.0)
Ĩ	hide	(ABC 2.46	IE8/B CH1	hide < AR_C_2_76	IT8 READ 1 (NOT USED)	hide	< AR_C_2_98	IR8 CH7
I	hide	XAR V 2 46	12010 0111	hide $> AR_V_2_76$		hide	> AR_V_2_98	
I	hide	AD M 2 46	rt m	hide < AR M 2 76	[1.0]	hide	< AR_M_2_98	(1.0)
I	hide	(AB D 2 46	0.0	hide < AR_D_2_76	(0.0)	hide	< AR_D_2_98	(0.0)
I	hide	(AR C 2 47	IF8/B CH2	bide (AD C 2.85	ITS UNDERDANCE & OVERDANCE BITS	hide	< AR_C_2_99	IR8 CH8
I	hide	AR V 2 47	LOID ONE	hide AR V 2.85	In ondera while a overa while bird	hide	> AR_V_2_99	
I	hide	(AR M 2 47	(1 M	hide AD M 2.85	n m	hide	< AR_M_2_99	(1.0)
I	hide		(0.0)		(1.0)	hide	< AR_D_2_99	(0.0)
I	hide	(AR_0_2_47				hide	< AR_C_2_100	IR8 UNDERRANGE & OVERRANGE BITS
I	hide	AD V 2 48	120/0 0113		IN OTHER STRIOS BITS	hide	> AR_V_2_100	
I	hide	AR M 2 48	(1 ())		(1 m)	hide	< AR_M_2_100	(1.0)
I	hide	(AR D 2 40	(1.0) (0.0)	111UE CAR_M_2_00	(1.0)	hide	< AR_D_2_100	(0.0)
I	hide	CAR_D_2_40		nide  < AR_D_2_86		hide	< AR_C_2_101	IR8 OTHER STATUS BITS
I	hide	AR V 2 40		hide < AR_C_2_91	IR8 READ T [NUT USED]	hide	> AR_V_2_101	
I	hide	/ AR_V_2_43	a w	hide > AH_V_2_91	4.0	hide	< AR_M_2_101	[1.0]
I	hide	(AR_M_2_45	(1.0) (0.0)	hide < AR_M_2_91	[1.0]	hide	< AR_D_2_101 🔽	(0.0)
	muc	IN AN D 6 43	10.0				-	
Ш	bide	( AD C 2 E0	IE OID CHE	Inde CAR_D_2_31	[0.0]			
l	hide bide	< AR_C_2_50	IE8/B CH5	hide $\langle AR_D_2 \rangle$	IR8 CH1	-		·
l	hide hide bide	< AR_C_2_50 > AR_V_2_50	IE8/В CH5	hide $\langle AR_0_2_3 \rangle$ hide $\langle AR_0_2_9 \rangle$ hide $\rangle AR_v_2_9 \rangle$	IR8 CH1			
	hide hide hide	< AR_C_2_50 > AR_V_2_50 < AR_M_2_50 < AR_D_2_50	1E8/B CH5 [1.0]	hide $\langle AR_B_2 = 31$ hide $\langle AR_C_2 = 92$ hide $\rangle AR_V = 2$	(1.0) (1.0)			
	hide hide hide hide	< AR_C_2_50 > AR_V_2_50 < AR_M_2_50 < AR_D_2_50 < AR_D_2_50	IE8/B CH5 (1.0) (0.0) IE8/B CH5	hide (AR_D_2_31 hide (AR_C_2_92 hide ) AR_V_2_92 hide (AR_M_2_92 hide (AR_M_2_92	(0.0) IR8 CH1 (1.0) (0.0)			
	hide hide hide hide hide	<pre>&lt; AR_C_2_50 &gt; AR_V_2_50 &lt; AR_M_2_50 &lt; AR_M_2_50 &lt; AR_D_2_50 &lt; AR_C_2_51 </pre>	IE8/8 CH5 (1.0) (0.0) IE8/8 CH6	hide (AA_D_2_31 hide (AA_C_2_92 hide ) AA_V_2_92 hide (AA_M_2_92 hide (AA_D_2_92 hide (AA_C_2_93)	(0-0) (1-0) (0-0) IR8 CH2			
	hide hide hide hide hide hide	<pre>&lt; AR_C_2_50 &gt; AR_V_2_50 &lt; AR_M_2_50 &lt; AR_D_2_50 &lt; AR_C_2_51 &lt; AR_C_2_51 &gt; AR_V_2_51 </pre>	iE8/95 CH5 (1.0) (0.0) IE8/95 CH6 (2.0)		(0.3) (1.0) (0.0) (R8 CH2			
	hide hide hide hide hide hide	<pre>&lt; AR_C_2_50 &gt; AR_V_2_50 &lt; AR_M_2_50 &lt; AR_D_2_50 &lt; AR_C_2_51 &gt; AR_V_2_51 &lt; AR_W_2_51 &lt; AR_M_2_51 &lt; AR_M_2_51 </pre>	1E8/8 CH5 (1.0) (0.0) 1E8/8 CH6 (1.0) 0.0		(0.0) (RB CH1 (0.0) (RB CH2 (1.0)			~
	hide hide hide hide hide hide hide	<pre>&lt; AR_C_2_50 &gt; AR_V_2_50 &lt; AR_M_2_50 &lt; AR_D_2_50 &lt; AR_C_2_51 &gt; AR_V_2_51 &lt; AR_M_2_51 &lt; AR_M_2_51 &lt; AR_D_2_51 &lt; AR_D_2_51 &lt; AR_D_2_51 </pre>	iE8/8 CHS (1.0) (0.0) IE8/8 CH6 (1.0) (0.0) IE8/8 CH7	hide         AR_0_2_31           hide         AR_C_2_92           hide         AR_W2_92           hide         AR_M2_92           hide         AR_M2_92           hide         AR_M2_92           hide         AR_M2_92           hide         AR_M2_92           hide         AR_M2_92           hide         AR_M2_93           hide         AR_M2_93	(0.5) (R6 CH1 (0.0) (R8 CH2 (1.0) (0.0) (0.0)			
	hide hide hide hide hide hide hide hide	<pre>&lt; AR_C_2_50 &gt; AR_V_2_50 &lt; AR_D_2_50 &lt; AR_D_2_50 &lt; AR_D_2_50 &lt; AR_C_2_51 &gt; AR_V_2_51 &lt; AR_M_2_51 &lt; AR_M_2_51 &lt; AR_D_2_51 &lt; AR_D_2_51 &lt; AR_C_2_52 </pre>	IE8(8 CH5 (1.0) (0.0) IE8(8 CH6 (1.0) (0.0) IE8(8 CH7	$ \begin{array}{l} \text{hide} < AR\_C\_2\_31\\ \text{hide} < AR\_C\_2\_92\\ \text{hide} > AR\_V\_2\_92\\ \text{hide} < AR\_M\_2\_92\\ \text{hide} < AR\_D\_2\_92\\ \text{hide} < AR\_C\_2\_93\\ \text{hide} > AR\_V\_2\_93\\ \text{hide} < AR\_M\_2\_93\\ \text{hide} < AR\_C\_2\_93\\ \text{hide} < AR\_C\_2\_93\\ \text{hide} < AR\_C\_2\_94\\ \end{array} $	(0.9) (R8 CH1 (0.0) (R8 CH2 (1.0) (0.0) (R8 CH3			
	hide hide hide hide hide hide hide hide	<pre>&lt; AR_C_2_50 &gt; AR_V_2_50 &lt; AR_M_2_50 &lt; AR_D_2_50 &lt; AR_C_2_51 &gt; AR_V_2_51 &lt; AR_M_2_51 &lt; AR_M_2_51 &lt; AR_C_2_51 &lt; AR_C_2_51 &lt; AR_C_2_52 &gt; AR_V_2_52 &lt; AR_V_2_52 </pre>	iE8/8 CHS (1.0) (0.0) IE8/8 CH6 (1.0) (0.0) IE8/8 CH7 0 00	$ \begin{array}{l} \text{inde} & \langle AR_{-}C_{-}2, 3 \rangle \\ \text{hide} & \langle AR_{-}V_{-}2, 92 \rangle \\ \text{hide} & \langle AR_{-}N_{-}2, 92 \rangle \\ \text{hide} & \langle AR_{-}0, 2, 92 \rangle \\ \text{hide} & \langle AR_{-}C_{-}2, 93 \rangle \\ \text{hide} & \langle AR_{-}V_{-}2, 93 \rangle \\ \text{hide} & \langle AR_{-}D_{-}2, 93 \rangle \\ \text{hide} & \langle AR_{-}D_{-}2, 93 \rangle \\ \text{hide} & \langle AR_{-}D_{-}2, 93 \rangle \\ \text{hide} & \langle AR_{-}C_{-}2, 94 \rangle \\ \text{hide} & \langle AR_{-}V_{-}2, 94 \rangle \\ \text{hide} & \langle AR_{-}V_{-}2, 94 \rangle \\ \end{array} $	(0.0) (R8 CH1 (0.0) (R8 CH2 (1.0) (0.0) (R9 CH3 (7.0)			
	hide hide hide hide hide hide hide hide	<pre>&lt; AR_C_2_50 &gt; AR_V_2_50 &lt; AR_D_2_50 &lt; AR_D_2_50 &lt; AR_C_2_51 &gt; AR_V_2_51 &lt; AR_C_2_51 &lt; AR_D_2_51 &lt; AR_D_2_51 &lt; AR_D_2_51 &lt; AR_C_2_52 &gt; AR_V_2_52 &lt; AR_M_2_52 &lt; AR_M_2_52 </pre>	IE8/8 CH5 (1.0) (0.0) IE8/8 CH6 (1.0) (0.0) IE8/8 CH7 (1.0) (0.0) IE8/8 CH7 (1.0) (0.0)	hide         AR_U_2_92           hide         AR_U_2_92           hide         AR_U_2_92           hide         AR_U_2_93	(0.9) (R8 CH1 (0.0) (R8 CH2 (1.0) (0.0) (R8 CH3 (1.9)			
	hide hide hide hide hide hide hide hide	<pre>&lt; AR_C_2_50 &gt; AR_V_2_50 &lt; AR_M_2_50 &lt; AR_D_2_50 &lt; AR_C_2_51 &gt; AR_V_2_51 &lt; AR_M_2_51 &lt; AR_D_2_51 &lt; AR_D_2_51 &lt; AR_D_2_52 &lt; AR_M_2_52 &lt; AR_M_2_52 &lt; AR_M_2_52 &lt; AR_M_2_52 &lt; AR_M_2_52 &lt; AR_M_2_52 </pre>	E8/8 CHS (1.0) (0.0) 16/9 CH6 (1.0) 16/9 CH6 (1.0) 16/9 CH6 10.0) 10.0) 10.0) 10.0) 10.0) 10.0)	$\begin{array}{llllllllllllllllllllllllllllllllllll$	(0.9) (RE CH1 (0.0) (RE CH2 (1.0) (RE CH2 (1.0) (RE CH3 (1.0) (0.0) (RE CH3			
	hide hide hide hide hide hide hide hide	<pre>&lt; AR_C_2_50 &gt; AR_V_2_50 &lt; AR_M_2_50 &lt; AR_C_2_51 &lt; AR_C_2_51 &gt; AR_V_2_51 &lt; AR_M_2_51 &lt; AR_M_2_51 &lt; AR_M_2_51 &lt; AR_D_2_51 &lt; AR_C_2_52 &lt; AR_V_2_52 &lt; AR_V_2_52 &lt; AR_V_2_52 &lt; AR_0_2_52 </pre>	IE8/8 CHS (1.0) (0.0) IE8/8 CH6 (1.0) IE8/8 CH7 (1.0) IE8/8 CH7 IE8/8 CH8	$ \begin{array}{llllllllllllllllllllllllllllllllllll$	(0.0) (1.0) (0.0) (0.0) (0.0) (0.0) (0.0) (R8 CH4			
	hide hide hide hide hide hide hide hide		IE8/8 CH5 (1.0) IE8/8 CH6 (1.0) IE8/8 CH7 (1.0) IE8/8 CH7 (1.0) IE8/8 CH8 (1.0) IE8/8 CH8 (1.0) IE8/8 CH8	$ \begin{array}{llllllllllllllllllllllllllllllllllll$	(0.0) (RB CH1 (1.0) (0.0) (RB CH2 (1.0) (0.0) (RB CH3 (1.0) (0.0) (RB CH4			
	hide hide hide hide hide hide hide hide	<ul> <li>AR_C_2_50</li> <li>AR_V_2_50</li> <li>AR_V_2_50</li> <li>AR_D_2_50</li> <li>AR_D_2_51</li> <li>AR_V_2_51</li> <li>AR_V_2_51</li> <li>AR_V_2_51</li> <li>AR_V_2_51</li> <li>AR_V_2_51</li> <li>AR_C_2_51</li> <li>AR_V_2_52</li> <li>AR_C_2_52</li> <li>AR_C_2_52</li> <li>AR_D_2_52</li> <li>AR_D_2_52</li> <li>AR_V_2_52</li> </ul>	IE8/8 CHS (1.0) (0.0) IE8/8 CH6 (1.0) IE8/8 CH7 (1.0) IE8/8 CH8 IE8/8 CH8 (1.0) IE8/8 CH8 IE8/8 CH8	$ \begin{array}{llllllllllllllllllllllllllllllllllll$	(0.0) (1.0) (0.0) (0.8) (0.8) (0.0) (0.0) (1.0) (0.0) (1.0) (1.0)			
	hide hide hide hide hide hide hide hide	<ul> <li>AR_C 2_50</li> <li>AR_V 2_50</li> <li>AR_V 2_50</li> <li>AR_V 2_50</li> <li>AR_D 2_50</li> <li>AR_D 2_51</li> <li>AR_V 2_51</li> <li>AR_V 2_51</li> <li>AR_V 2_51</li> <li>AR_V 2_51</li> <li>AR_V 2_52</li> <li>AR_V 2_52</li> <li>AR_V 2_52</li> <li>AR_V 2_52</li> <li>AR_V 2_52</li> <li>AR_V 2_53</li> </ul>	IE8/8 CH5 (1.0) (0.0) IE8/8 CH5 (1.0) (0.0) IE8/8 CH7 (1.0) (0.0) IE8/8 CH8 (1.0) (0.0) IE8/8 CH8 (1.0) (0.0) (0.0)	$ \begin{array}{llllllllllllllllllllllllllllllllllll$	(0.0) (R8 CH1 (0.0) (R8 CH2 (1.0) (0.0) (R8 CH3 (1.0) (R8 CH4 (1.0) (0.0)			
	hide hide hide hide hide hide hide hide	<ul> <li>AR_C 2 50</li> <li>AR_V 2 50</li> <li>AR_V 2 50</li> <li>AR_V 2 50</li> <li>AR_D 2 50</li> <li>AR_D 2 50</li> <li>AR_V 2 51</li> <li>AR_V 2 51</li> <li>AR_V 2 51</li> <li>AR_V 2 51</li> <li>AR_V 2 52</li> <li>AR_V 2 53</li> <li>AR_V 2 53</li> <li>AR_V 2 54</li> <li>AR_V 2 54</li> <li>AR_V 2 54</li> </ul>	IE8/8 CHS (1-0) (0-0) IE8/8 CH6 (1-0) IE8/8 CH7 (1-0) (0-0) IE8/8 CH7 IC0) IE8/8 CH8 IC0) IE8/8 CH8 IC0) IE8/8 CH8 IC0) IC0) IC0) IC0) IE8/8 CH8 IC0) IC0	$\begin{array}{llllllllllllllllllllllllllllllllllll$	(I.0) (I			
	hide hide hide hide hide hide hide hide	<ul> <li>AR_C 2_50</li> <li>AR_V 2_50</li> <li>AR_V 2_50</li> <li>(AR_D 2_50</li> <li>(AR_D 2_50</li> <li>(AR_C 2_51</li> <li>&gt;AR_V 2_51</li> <li>(AR_D 2_51</li> <li>(AR_D 2_51</li> <li>(AR_D 2_51</li> <li>(AR_D 2_51</li> <li>(AR_D 2_52</li> <li>(AR_C 2_52</li> <li>(AR_C 2_52</li> <li>(AR_C 2_53</li> <li>&gt;AR_V 2_53</li> <li>&gt;AR_V 2_53</li> <li>(AR_D 2_52</li> <li>(AR_D 2_52</li> <li>(AR_D 2_53</li> <li>&gt;AR_V 2_54</li> <li>&gt;AR_V 2_54</li> </ul>	IE8/8 CHS [1:0] [0:0] IE8/8 CH5 [1:0] [0:0] IE8/8 CH7 [1:0] IE8/8 CH9 [1:0] IE8/8 CH9 [1:0] IE8/8 CH9 [1:0] IE8/8 CH9 [1:0] IE8/8 CH9 [1:0] IE8/8 CH9 [1:0] IE8/8 CH5 [1:0] IE8/8 CH5 [1:0]	$ \begin{array}{llllllllllllllllllllllllllllllllllll$	(I.0) (I			
	hide hide hide hide hide hide hide hide	<ul> <li>AR C 2 50</li> <li>AR V 2 50</li> <li>AR M 2 50</li> <li>AR M 2 50</li> <li>AR M 2 50</li> <li>AR M 2 51</li> <li>AR V 2 51</li> <li>AR V 2 51</li> <li>AR V 2 51</li> <li>AR M 2 51</li> <li>AR M 2 51</li> <li>AR V 2 52</li> <li>AR V 2 53</li> <li>AR V 2 53</li> <li>AR C 2 54</li> <li>AR V 2 54</li> <li>AR V 2 54</li> <li>AR M 2 51</li> </ul>	IE8/8 CHS (1-0) (0-0) IE8/8 CH6 (1-0) IE8/8 CH7 (1-0) (0-0) IE8/8 CH7 (1-0) IE8/8 CH8 II.0) IE8/8 CH8 II.0)	$ \begin{array}{llllllllllllllllllllllllllllllllllll$	(I.0) (I			

Figure 6-52. MODBUS\_M Block Group 2 Analog Read RPT Example

Figure 6-53 shows the used write addresses for Group 2 (41201-41245, Analog Write).

hide	< AW_C_2_1	IB16 FILTER TIME & COUNTER BITS
hide	< AW_V_2_1	IB16.WRITE.OUT_1
hide	< AW_M_2_1	(1.0)
hide	< AW_C_2_16	OV16 CHANNELS
hide	< AW_V_2_16	OV16.CHANNELS.OUT_1
hide	< AW_M_2_16	(1.0)
hide	< AW_C_2_31	OW8 CHANNELS
hide	< AW_V_2_31	OW8.CHANNELS.OUT_1
hide	< AW_M_2_31 👻	(1.0)

Figure 6-53. MODBUS\_M Block Group 2 Analog Write RPT Example

Figure 6-54 shows all of the used write addresses for Group 3 (41246-41290, Analog Write)

hide	< AW_C_3_1	IE8/B FULL RANGE & CONFIGURE BITS
hide	< AW_V_3_1	IE8/B.WRITE.OUT_1
hide	< AW_M_3_1	(1.0)
hide	< AW_C_3_16	OE4/B CH1
hide	< AW_V_3_16	OE4/B.AO_1.CALCULATE
hide	< AW_M_3_16	(1.0)
hide	< AW_C_3_17	OE4/B CH2
hide	< AW_V_3_17	OE4/B.AO_2.CALCULATE
hide	< AW_M_3_17	(1.0)
hide	< AW_C_3_18	OE4/B CH3
hide	< AW_V_3_18	OE4/B.AO_3.CALCULATE
hide	< AW_M_3_18	(1.0)
hide	< AW_C_3_19	OE4/B CH4
hide	< AW_V_3_19	OE4/B.AO_4.CALCULATE
hide	< AW_M_3_19	(1.0)
hide	< AW_C_3_20	OE4/B OUTPUT ENABLE BITS
hide	< AW_V_3_20	0E4/B.WRITE1.0UT_1
hide	< AW_M_3_20	(1.0)
hide	< AW_C_3_21	OE4/B FULL RANGE & CONFIGURE BITS
hide	< AW_V_3_21	0E4/B.WRITE2.0UT_1
hide	< AW_M_3_21	(1.0)
hide	< AW_C_3_31	IT8 UNITS, FILTER & CAL BITS
hide	< AW_V_3_31	IT8.WRITE1.0UT_1
hide	< AW_M_3_31	(1.0)
hide	< AW_C_3_32	IT8 TC TYPE BITS
hide	< AW_V_3_32	IT8.WRITE2.0UT_1
hide	< AW_M_3_32	(1.0)
hide	< AW_C_3_33	IT8 TC TYPE BITS
hide	< AW_V_3_33	IT8.WRITE3.0UT_1
hide	< AW_M_3_33 🖵	(1.0)



Figure 6-55 shows all of the used write addresses for Group 4 (41291-41294, Analog Write).

hide	< AW_C_4_1	IR8 UNITS, MODE, FILTER & CAL BITS
hide	< AW_V_4_1	IR8.WRITE1.0UT_1
hide	< AW_M_4_1	(1.0)
hide	< AW_C_4_2	IR8 RTD TYPE BITS
hide	< AW_V_4_2	IR8.WRITE2.OUT_1
hide	< AW_M_4_2	(1.0)
hide	< AW_C_4_3	IR8 RTD TYPE BITS
hide	< AW_V_4_3	IR8.WRITE3.OUT_1
hide	< AW_M_4_3	(1.0)

Figure 6-55. MODBUS\_M Block Group 4 Analog Write RPT Example

# ProSoft Modbus Interface (3170-MBS) Module



In addition to the individual I/O module read and write addresses, there are several status read addresses provided by the 3170-MBS Interface module. These status words can be used to monitor the condition of the I/O modules via the GAP application. See Figure 6-56 for 3170-MBS Status Information addresses from the 3170-MBS User Manual.

Adapter Status	Word 4012	1
Bit Description	Bit	Explanation
	0	This bit is set (1) when an error is detected in slot position 0.
	1	This bit is set (1) when an error is detected in slot position 1.
	2	This bit is set (1) when an error is detected in slot position 2.
I/O Module Fault	3	This bit is set (1) when an error is detected in slot position 3.
	4	This bit is set (1) when an error is detected in slot position 4.
	5	This bit is set (1) when an error is detected in slot position 5.
	6	This bit is set (1) when an error is detected in slot position 6.
	7	This bit is set (1) when an error is detected in slot position 7.
I/O Last State	8	= 1 for hold last state = 0 for off
	9 - 15	Not used set to 0

Module Status Words Address 40122 to 40129

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	97	Statu	s	Total Words	Re	ad V	Vord	s			Тур	e Ide	ntity			

Module Information	
3170-MBS Information	Address
3170-MBS Product Revision Level	40154
3170-MBS Product Batch Number	40155
Modbus Function Counters	
Modbus Port Function Code Counter	Address
Function Code 1	40156
Function Code 2	40157
Function Code 3	40158
Function Code 4	40159
Function Code 5	40160
Function Code 6	40161
Function Code 15	40162
Function Code 16	40163
Modbus	
Modbus Status	Address
Modbus Port - Responses to Host	40171
Modbus Port - No Responses to Host	40172
Modbus Port - Last Detected Error Condition	40173

Figure 6-56. 3170-MBS Status Information Addresses

Addresses 40121 to 40129 are all status words that represent 16 individual Boolean output conditions. For the GAP application to read the individual bits associated with the 16 bit words in the status addresses above, an A\_TO\_16B GAP Block is used. These blocks convert the 16 bit word from the addresses in the MODBUS\_M group 1 entries to individual Boolean states that can be used by the GAP application. See Figure 6-57 for example of setup of the discrete Status Word GAP blocks used to read the 3170-MBS memory map.

Adapter	Module 1	Module 2	Module 3	Module 4
Status word	Status word	Status word	Status Word	Status Word
ADAPTRSTAT	HIBS MODEL STAT	MBS MOD2 STAT	MBS MOD3 STAT	MBS MOD4 STAT
AD2 MAIN HODRUSAR V 1 1-00-IN 1	AT2 BAIN HODEUSAR V 1 2-00-N 1	ATZ HAIN HODAUSAR V 1 3-00-IN 1	ATZ HAN HODRUSAR V 1 4-00-N 1	AD2 MAIN HODRUSAR V 15-00-IN 1
	HODILE 1 TYPE ID -COUL 1 1		UCDILESTYREID COUL 1	NULL NULL OUT 2.1
NODULE 2 FAULT - COUL 2 1			HODULESTYRE D-COULS 1	
HODULE3EAULT-COULS 1				NODILLEATYREID -COULS 1
HODULEA RAWT-CON A 1			NODULETTYRED CON ( )	
HODULESFAULT-COM S 1				
NODULESTINGT CON 6 1				
NODULESTANCE OUT_S_1				
NODULETINCT COM_T_OUT_9_1			NODULESTIVE D COM TO UT_9_1	HODULE (TITLE DOWOUT_9_1
OUT_10_1				
OUT_11_1	OUT_11_1	OUT_11_1	OUT_11_1	OUT_11_1
10-16 NOT 05ED -COM_10_1 OUT_12_1	OUT_12_1	0000122 READ VIOLADS -COM_10_1	OUT_12_1	OUT_12_1
NOT USED -COM_11_1 OUT_13_1	MODULE1 READ WORDS-COM_11_1 OUT_13_1	DUT_13_1	DUT_13_1	MODULE 4 READ WORDS - COM_11_1 DUT_13_1
NOT 05ED -COM_12_1 OUT_14_1	OUT_14_1	DUT_14_1	DUT_14_1	OUT_14_1
NOT USED COM_13_1 OUT_15_1	NODULE 1 TOTAL WORDS -COM_13_1 OUT_15_1	DUT_15_1	MODULES TOTAL WORDS - COM_13_1 DUT_15_1	DUT_15_1
NOT USED -COM_14_1 OUT_16_1	MODULE 1 BAD DATA -COM_14_1 OUT_16_1	NODULE 2 BAD DATA -CON_14_1 OUT_16_1	MODULE3 BAD DATA -COM_14_1 OUT_16_1	MODULE 4 BAD DATA -COM_14_1 OUT_16_1
NOT USED -CON_15_1	MODULE 1 FAULT OR -COM_15_1	MODULE2 FAULT OR -COM_15_1	MODULE3 FAULTOR -COM_15_1	MODULE 4 FAULT OR - COM_15_1
NOT USED -CON 15 1 A TO 168 5	MODULE 1 EMPTY -COM 16 1 A TO 168 S	MODULE 2 EMPTY -COM_16_1 A TO 168 S	MODULE3EMPTY-COM_15_1 A TO 168 5	NODULE 4 EMPTY-COM_16_1 A TO 168 S
MBS MOD5 STAT	MODE STAT	MBS MOD7 STAT	MBS MOD8 STAT	
(LSB) -SENSE	(LSB) -SENSE	(LSE) -SENSE	(LSB) SENSE	From MODDUO M
A02_MAIN.MODBUSAR_V_1_6	AD2_MAIN.MODBUSAR_V_17 - 0 - N_1 OUT 2 1	AD2_MAIN.MODBUSAR_V_1_8-00-IN_1 OUT 2.1	AZZ_MAIN.MODBUSAR_V_1.9-00-00-001-011	From MODBUS_M
MODULESTYPE ID - COM_1_1 OUT 3 1	MODULESTYPE ID -COM_1_1 OUT 3 1N	MODULE? TYPE ID -COM_1_1 OUT 3 1	MODULESTYPE ID -COM_1_1 OUT 3 1	(Address 40129)
MODULES TYPE ID - COM_2_1	MODULES TYPE ID -COM_2_1 OUT 4 1	MODULET TYPE ID -COM_2_1	MODULES TYPE ID -COM_2_1	
MODULESTYPE ID - COM_3_1	MODULESTYPE ID -COM_3_1 OUT 5 1	MODULE? TYPE ID -COM_3_1 OUT 5 1	MODULESTYPE ID -COM_3_1 OUT & 1	
MODULESTYPE ID - COM_4_1	MODULESTYPE ID -COM_4_1 OUT_5_1	MODULET TYPE ID - COM_4_1	MODULES TYPE ID -COM_4_1 OUT_6_1	
MODULESTYPE ID -COM_5_1	MODULESTYPE ID -COM_S_1	MODULE? TYPE ID -COM_S_1	MODULESTYPE ID -COM_S_1	
MODULES TYPE ID -COM_6_1	MODULES TYPE ID -COM_6_1	MODULET TYPE ID -COM_6_1	MODULES TYPE ID -COM_6_1	
MODULES TYPE ID - COM_7_1	MODULESTYPEID -COM_7_1	MODULE? TYPE ID -COM_7_1	MODULES TYPE ID -COM_7_1	Discrete Outputs
MODULES TYPE ID - COM_8_1	MODULES TYPE ID -COM_8_1	MODULE? TYPE ID -COM_8_1	MODULES TYPE ID -COM_S_1	
MODULES READ WORDS-COM_9_1	MODULES READ WORDS-COM_9_1	HODULE? READ WORDS -COM_9_1	MODULES READ WORDS - COM_9_1	(
MODULES READ WORDS -COM_10_1	MODULES READ WORDS-COM_10_1	MODULET READ WORDS - COM_10_1	MODULES READ WORDS - COM_10_1	
MODULES READ WORDS-COM_11_1	MODULES READ WORDS-COM_11_1	HODULE? READ WORDS -COM_11_1	MODULES READ WORDS - COM_11_1	
MODULES READ WORDS-COM_12_1	MODULES READ WORDS-COM_12_1	MODULET READ WORDS-COM_12_1	MODULES READ WORDS -COM_12_1	
MODULES TOTAL WORDS-COM_13_1	MODULE 6 TOTAL WORDS -COM_13_1	MODULE? TOTAL WORDS - COM_13_1	MODULES TOTAL WORDS - COM_13_1	
MODULES BAD DATA -COM_14_1	MODULE6 BAD DATA -COM_14_1	NODULET BAD DATA-CON_14_1	NODULES BAD DATA -CON_14_1	/
MODULES FAULT OR - COM_15_1	MODULES FAULT OR -COM_15_1	NODULE? FAULT OR -CON_15_1	MODULES FAULT OR - CON_15_1	/
MODULES EMPTY-COM_16_1	MODULES EMPTY -CON 15 1	NODULET ENPTY-CON 16 1	MODULES EMPTY-COM 16 1	
LA 10 168 [ 6 ]	A 10 168   5	LA 10 168 [5]		
Module 5	Module 6	Module 7	Module 8	
Status Word	Status Word	Status Word	Status Word	

Figure 6-57. Example of 3170-MBS Memory Map Discrete Read GAP Blocks

The remaining Adapter status words (40154 - 40163 and 40171 - 40173) are all 16 bit words and can be handled by the GAP application as an analog values. An A\_NAME block is used to connect the specific status function with the addresses entered in the MODBUS\_M block. See Figure 6-58 for an example of the 3170-MBS Status Word monitoring.



Figure 6-58. Example of 3170-MBS Memory Map Analog Read GAP Blocks





In this example, the 1794-IB16 module is plugged into a 1794-TB3S base. See Figure 6-59 for example of 1794-IB16 module wiring.

DIST Allen-Bradle	RIBUTED I/O y FLEX I/O 1794-IB1	16		→ To 24VDC Com
DISC	RETE INPUT			→ To +24VDC
	(-COM)	B16		
	(+24VDC)	C34		
	DI (+)	A0	$\vdash$	
MBI.A1.A02.G1.N1_BI_01	(-COM)	B17	$\vdash$	
	(+24VDC)	C35		
	DI (+)	A1		<u></u> • • •
MBI.A1.A02.G1.N1_BI_02	(-COM)	B18		
	(+24VDC)	C36		
	DI (+)	A2		
MBI.A1.A02.G1.N1_BI_03	(-COM)	B19		
	(+24VDC)	0.37		
	DI (+)	A3 B20		
MBI.A1.A02.G1.N1_BI_04	(-COM)	620		
	(+24VDC)	0.38		
	DI (+)	P01		
MBI.A1.A02.G1.N1_BI_05	(-COM)	B21		
	(+24VDC)	039		
MPLA1 A02 C1 N1 PL 06		A3		
WIDI.A1.A02.G1.N1_DI_00	(-COM)	640		
	(+24VDC)	040		
MPLA1 A02 C1 N1 PL 07		P23		
WDI.A1.A02.01.W1_DI_0/	(+24)/DC)	C41		
	(+24VBC)	Δ7		
MBLA1 A02 G1 N1 BL 08	(-COM)	B24		
	(+24VDC)	C42		
	DI (+)	A8		
MBLA1.A02.G1.N1 BL 09	(-COM)	B25		
	(+24VDC)	C43		
	DI (+)	A9		
MBI.A1.A02.G1.N1 BI 10	(-COM)	B26		
	(+24VDC)	C44		
	DI (+)	A10		
MBI.A1.A02.G1.N1_BI_11	(-COM)	B27		
	(+24VDC)	C45		
	DI (+)	A11		
MBI.A1.A02.G1.N1_BI_12	(-COM)	B28		
	(+24VDC)	C46		-
	DI (+)	A12		
MBI.A1.A02.G1.N1_BI_13	(-COM)	B29		
	(+24VDC)	C47		_
	DI (+)	A13		
MBI.A1.A02.G1.N1_BI_14	(-COM)	B30		
	(+24VDC)	C48		
	DI (+)	A14		
MBI.A1.A02.G1.N1_BI_15	(-COM)	B31		
	(+24VDC)	C49		
	DI (+)	A15		
MBI.A1.A02.G1.N1_BI_16	(-COM)	B32		
	(+24VDC)	C50		
	(-COM)	B33		
1	(+24VDC)	C51		

Figure 6-59. Example of 1794-IB16 Module Wiring

The 1794-IB16 memory map indicates that there are two read addresses and one write address. See Figure 6-60 for memory map of Allen-Bradley 1794-IB16 Discrete input module.

#### Memory Map

Dec.	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Read 0	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
Read 1	C = 16 bit Counter Value of Input 15															
Write	N us	ot ed	CF	CR	Not used				FT 12–15			FT 00–11				
Where: D = Data Input – 0 = input off, 1 = input on C = Counter value for input 15 FT = Input Filter Time CR = Counter Reset CF = Counter Fast – where 1 = Fast Input (raw) data, 0 = Standard Input filtered data NOTE: C, CR and CF not available when used with any series 1794-ASB or 1794-ASB2 Remote I/O Adapter Modules																

Figure 6-60. 1794-IB16 Memory Map

In this example, this module was set up with filter times of 256us for all inputs, Counter Reset set to off, and Counter set to standard input filtered data. See Figure 6-61 for input filter time bit map.

Bits			Description				
02	01	00	Filter Time for Inputs 00–11(00–13)	Selected			
05	04	03	Filter Time for Inputs 12–15(14–17)				
0	0	0	Filter Time 0 (default)	256µs			
0	0	1	Filter Time 1	512µs			
0	1	0	Filter Time 2	1ms			
0	1	1	Filter Time 3	2ms			
1	0	0	Filter Time 4	4ms			
1	0	1	Filter Time 5	8ms			
1	1	0	Filter Time 6	16ms			
1	1	1	Filter Time 7	32ms			

#### **Input Filter Times**

Figure 6-61. 1794-IB16 Input Filter Time Bit Map

In this example only one read address (41001) is monitored. Again, an A\_TO\_16B block is used to convert the word to 16 individual discrete input states. The memory map for this module requires discrete bits to be set for the filter times and counter functions in the write address. This is done by using an B16\_TO\_A block to write to the 1794-IB16 write address 41201. See Figure 6-62 for example of 1794-IB16 Read and Write GAP blocks



Figure 6-62. Example of 1794-IB16 Read and Write GAP Blocks
## Allen-Bradley 24 Vdc Sink Output (1794-OV16) Module



In this example, the 1794-OV16 is connected to a Woodward 16 channel relay module. See Figure 6-63 for example of 1794-OV16 module wiring.

r			, ,	+28	VDC	TB49 +	
DIS	TRIBUTED I/O			28	COM	TDEO	ב ר
Allen-Bradle	V FI FX I/O 1794-OV1	6		20	14.22	1850 -	
	,,	•			J1-24	1	Woodward
DISC	RETE OUTPUT			Г		1 10	6 Channel Relav
	(-COM)	B16			J1-21	-	P/N 5441-691
	(+24VDC)	C34			31-22	1	1/11/0441-001
	DO (+)	A0	1	+	J1-19	K1	Or
MBI.A1.A02 G1.N2_BO_01	(-COM)	B17					P/N 5441-419
	(+24VDC)	C35		-	14.40		
	DO (+)	A1			J1-10	K2	
MBI.A1.A02 G1.N2_B0_02	(-COM)	B18					
	(+24VDC)	C36			11-17		
	DO (+)	A2	-		51-17	K3	
MBI.A1.A02 G1.N2_B0_03	(-COM)	B19					
	(+24VDC)	037			J1-16		
	DO (+)	A3				1 K4	
MBLA1.A02 G1.N2_BO_0	(-COM)	B20	-				
	(+24VDC)	0.30	-		J1-15	VE	
	DO (+)	A4				1 42	
MBLAT A02 G1.142_B0_00	(+24)/DC)	C30	•				
	(124VBC)	45			J1-14	Ke	
MBLA1 A02 G1 N2 BO 08	(-COM)	B22	1				
	(+24VDC)	C40	1				
	DO (+)	A6			J1-13	K7	
MBI.A1.A02 G1.N2 BO 07	(-COM)	B23					
	(+24VDC)	C41					
	DO (+)	A7	<b> </b>		J1-12	K8	
MBI.A1.A02 G1.N2_BO_08	(-COM)	B24	1				
	(+24VDC)	C42			14.44		
	DO (+)	A8			J1-11	K9	
MBI.A1.A02 G1.N2_BO_09	(-COM)	B25					
	(+24VDC)	C43			11-10		
	DO (+)	A9			31-10	K10	
MBI.A1.A02 G1.N2_B0_10	(-COM)	B26	-				
	(+24VDC)	C44			J1-9	K11	
	D0 (+)	A10				1	
MBLALAUZ GLNZ_BO_TT	(+24)(DC)	D27	-				
	(+24VBC)	A11			J1-8	K12	
MBI 41 402 G1 N2 BO 12	(COM)	B28	-				
	(+24VDC)	C46					
	DO (+)	A12			J1-7	K13	
MBLA1.A02 G1.N2 BO 13	(-COM)	B29	1				
	(+24VDC)	C47	1				
	DO (+)	A13			J1-6	K14	
MBI.A1.A02 G1.N2_BO_1	(-COM)	B30					
	(+24VDC)	C48	1				
	DO (+)	A14			J1-5	K15	
MBI.A1.A02 G1.N2_BO_15	(-COM)	B31					
	(+24VDC)	C49			14.4	1/16	
	DO (+)	A15			J1-4	10	
MBLA1.A02 G1.N2_B0_16	(-COM)	B32	1			L	
	(+24VDC)	C50					
	(-COM)	B33	-		To 24VDC	COM	
	(+24VDC)	C51	J		→ 10 +24VD	C	

Figure 6-63. Example of 1794-OV16 Module Wiring

The memory map indicates that there are zero read addresses and one write address. See Figure 6-64 for memory map of 1794-OV16 module.

## **Memory Mapping**

Bit⇒ Word <b></b> ↓	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Read	Not used															
Write	015	014	O13	012	011	O10	09	08	07	O6	O5	O4	O3	02	01	00
Where:	0 = Ou	itput va	alue			-										

Figure 6-64. 1794-OV16 Module Memory Map

To write the discrete output bits for the 1794-OV16 module, a B16\_TO\_A block is used. See Figure 6-65 for example of GAP write block configuration.



Figure 6-65. Example of 1794-OV16 GAP Write Blocks

## Allen-Bradley Relay Output (1794-OW8) Module



In this example, the relay outputs are individually fused to protect the module. See Figure 6-66 for example of 1794-OW8 module wiring.





00 00 00

The memory map indicates that there is one read address and one write address. See Figure 6-67 for memory map of 1794-OW8 module.

	inage	Tak		CIII	J' J' J'	Map										
	Word		Mem Ma	ory p	D (0	ec. B ctal E	lits Bits)			Des	cripti	on			For	mat
	Read		Inpu	ıt	00-	15 (00	)–17)	No	ot used	d – res	erved					
	Write		Outp	ut		00–0	7	Re co co	elay O rrespo rrespo	utput o onds to onds to	data – ( o outpu o outpu	00 it 0, 01 it 1, et	l c.	0 = 1 =	Outpu Outpu	ıt off ıt on
					-80	15 (10	0–17)	No	ot used	d						
			-	-	-	-	-	-		-	-	-				
	Dec.	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01
Ī	(Octal)	17	16	15	14	13	12	11	10	07	06	05	04	03	02	01
	Write			No	ot used	- set i	to O			07	06	05	04	03	02	01
	Write			No	t used	- set i	to O			07	06	05	04	03	02	01

## Image Table Memory Map

Where O = Output number

When bit = 0, output is off; when bit =1, output is on

Figure 6-67. 1794-OW8 Module Memory Map

To write the discrete output bits for the 1794-OW8 module, again a B16\_TO\_A block is used. Since there are only eight outputs, only the first eight block inputs are used. See Figure 6-68 for example of GAP write block configuration.



Figure 6-68. Example of 1794-OW8 GAP Write Blocks

## Allen-Bradley Analog Input (1794-IE8/B) Module



In this example, loop powered transducers are shown. See Figure 6-69 for example of 1794-IE8/B module wiring.

DIST Allen-Bradley ANA	RIBUTED I/O / Flex I/O 1794-Ie8/ Alog Input	В	[		► To 24COM
	(-COM)	B16			▶ To +24VDC
	(+24)/DC)	C34			$\frown$
		 			- (4-20mA +
MBLA1 A02 G1 N4 AL 01		B17			Xducer
MDI.AT.A02.01.144_AI_01	(+24)/DC)	C35			<u> </u>
	(124000)	Δ1			
Not Lleed	(COM)	R18			
Not Obeu	(+24)/DC)	C36			$\frown$
	(124VDC) AI (+)	Δ2			- (4-20mA +
MBI 41 402 G1 N4 41 02	(-COM)	B19			Xducer
MDI.A1.A02.01.14_AI_02	(+24)/DC)	C37		4	_
	(124780) VI (+)	Δ3			
Not Lleed	(-COM)	B20			
Not Osed	(+24)/DC)	C38			$\sim$
		0.30			- (4-20mA) +
MRI A1 A02 G1 N4 AL 03		P21			Xducer
MDI.A1.A02.01.N4_AI_00	(+24)/DC)	C30			$\smile$
	(+24VDC)	039			
Not Lload		AU PDD			
Not Used	(-COM)	D22			_
	(+24VDC)	040			- (4-20mA) +
		A0			Xducer
WIDI.A1.A02.G1.IN4_AI_04	(-COM)	D23			$\smile$
	(+24VDC)	A7			
Not Llood		R/			
Not Used	(-COM)	D24			
		 			- (4-20mA) +
		R0			Xducer
WIDI.AT.AU2.GT.IN4_AI_05	(-COM)	D23			$\smile$
	(+24VDC)	043			
Not Llood		A9 D26			
Not Used	(-COM)	620 C44			~
	(+24VDC)	044 A10			- (4-20mA) +
		R10			Xducer
WIDI.AT.AU2.GT.IN4_AI_00	(-COM)	D21			$\smile$
	(+24VDC)	045 A11			
Not Llood		P29			
Not Used	(+24)/DC)	D20			$\sim$
	(+24VDC)	A12			- (4-20mA) +
MRI A1 A02 G1 N4 AL 07		R20			Xducer
MDI.A1.A02.01.N4_AI_0/	(+24)/DC)	C47			$\smile$
	(124000)	A13			
Not Llood	(COM)	R30			
Not Used	(+24)/DC)	C48			
	(127700) AI (+)	Δ14		15	- (4-20mA +
MRI 41 402 G1 N/4 41 09		R14 R31			Xducer
WDI.AT.A02.GT.IN4_AI_08	(124)(DC)	C40		60	$\smile$
	(124000)	A15			
Not Llood		A IU D22			
NUL USEU	(+24)/DC)	C50			
	(+24VDC)	D22			
	(-COIVI)	000			

Figure 6-69. Example of 1794-IE8/B Module Wiring

The memory map indicates that there are nine read addresses and one write address. See Figure 6-70 for the input memory map and Figure 6-71 for the output memory map for the 1794-IE8/B module.

Input I	Map															
Bit⇒ Word ↓	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
							R	ead								
0	S					A	nalog	Input	Value	for Ch	annel	0				
1	S					A	nalog	Input	Value	for Ch	annel	1				
2	S					A	nalog	Input	Value	for Ch	annel	2				
3	S					A	nalog	Input	Value	for Ch	annel	3				
4	S					A	nalog	Input	Value	for Ch	annel	4				
5	S					A	nalog	Input	Value	for Ch	annel	5				
6	S					A	nalog	Input	Value	for Ch	annel	6				
7	S					A	nalog	Input	Value	for Ch	annel	7				
8	PU			Not us	ed - s	et to O	)		U7	U6	U5	U4	U3	U2	U1	U0
Where:	S = 3 U = PU =	Sign bi Underi = Powe	it (in 2 range er up	's com bits bit	pleme	nt)										

Figure 6-70. 1794-IE8/B Input Module Memory Map

**Underrange bits (U)**—These bits are set (1) when the input channel is below a preset limit as defined by the configuration selected. U0 (bit 00) corresponds to input channel 0 and U1 (bit 01) corresponds to input channel 1, etc. **Power Up (unconfigured state) bit (PU)**—This bit is set (1) when the configuration word is all zeroes (0) due to a reset (adapter power cycle or module insertion) or a cleared configuration word (all 0). When this bit is set (1), the module status indicator flashes.

### **Output Map**

Bit⇒ Word∜	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
							Wr	ite								
0	C7	C6	C5	C4	C3	C2	C1	C0	F7	F6	F5	F4	F3	F2	F1	F0
Where:	C = C F = Fi	onfigu ıll ranı	re sele ge bit	ect bit												

#### **Range Selection Bits**

•																
Channel No.	Ch	. 0	Ch	. 1	Ch	. 2	Ch	. 3	Ch	. 4	Ch	. 5	Ch	. 6	Ch	. 7
	F0	C0	F1	C1	F2	C2	F3	C3	F4	C4	F5	C5	F6	C6	F7	C7
Decimal Bits	00	08	01	09	02	10	03	11	04	12	05	13	06	14	07	15
0-10V dc/0-20mA	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
4-20mA	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
-10 to +10V dc	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Off <sup>1</sup>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C = Configure selec	t bit															

F = Full range bit

<sup>1</sup> When configured to Off, individual input channels will return 0000H.

Figure 6-71. 1794-IE8/B Output Module Memory Map

In this example, the write block is set up with Range Select bits for all channels set to 0-21mA. The read block is set up to be able to read the status of the underrange bits for all channels and the Power Up bit (PU). See Figure 6-72 for example of 1794-IE8/B Read and Write GAP blocks.



Figure 6-72. Example of 1794-IE8/B Read and Write GAP Blocks

To read and scale the analog input words for the 1794-IE8/B module, CALCULATE blocks were used. For the GAP block to convert the raw counts read from the 1794-IE8/B module to engineering units, the relationship between raw counts and engineering units needs to be specified in the CALCULATE block. The raw count to milliamp relationship can be found in the Allen-Bradley manual 1794-6.5.2. See Figure 6-73 for Analog Data Format Table. The table specifies counts in hexadecimal form and the CALCULATE block requires the RAW\_LOW and RAW\_HIGH fields to be entered in decimal form. Under the 0-20mA column in the Analog Data Format Table, 21mA is equivalent to 7FF8 hexadecimal. Converting 7FF8 to decimal equals 32760 Counts RAW\_HIGH. In this example the CALCULATE block scales the 0-32760 counts for 0-21mA (engineering units) for the module. The output of the CALCULATE block is in engineering units (milliamps) and is used by the GAP application as the milliamp value read from the 1794-IE8/B module. See Figure 6-74 for example of 1794-IE8/B GAP CALCULATE scaling blocks.

0	A com A Mada	A com A Mada	Vallana (10	+10 Vol	t Mode	0-10 Volt
Current (mA)	4-20mA Mode	U-20MA Mode	voitage (v)	Input	Output	Mode
			-10.50	8000	8000	
0.00		0000	-10.00	8620	8618	
1.00		0618	-9.00	9250	9248	
2.00		0C30	-8.00	9E80	9E78	
3.00		1248	-7.00	AAB0	AAA8	
4.00	0000	1860	-6.00	B6E0	B6D8	
5.00	0787	1E78	-5.00	C310	C310	
6.00	0F0F	2490	-4.00	CF40	CF40	
7.00	1696	2AA8	-3.00	DB70	DB70	
8.00	1E1E	30C0	-2.00	E7A0	E7A0	
9.00	25A5	36D8	-1.00	F3D0	F3D0	
10.00	2D2D	3CF0	0.00	0000	0000	0000
11.00	34B4	4310	1.00	0C30	0C30	0C30
12.00	3C3C	4928	2.00	1860	1860	1860
13.00	43C3	4F40	3.00	2490	2490	2490
14.00	4B4B	5558	4.00	30C0	30C0	30C0
15.00	52D2	5B70	5.00	3CF0	3CF0	3CF0
16.00	5A5A	6188	6.00	4920	4928	4928
17.00	61E1	67A0	7.00	5550	5558	5558
18.00	6969	6DB8	8.00	6180	6188	6188
19.00	70F0	73D0	9.00	6DB0	6DB8	6DB8
20.00	7878	79E8	10.00	79E0	79E8	79E8
21.00	7FFF	7FF8	10.50	7FF0	7FF8	7FF8





Figure 6-74. Example of 1794-IE8/B GAP CALCULATE Scaling Blocks

## Allen-Bradley Analog Output (1794-OE4/B) Module



See Figure 6-75 for example of 1794-OE4/B module wiring.





Output Man

The memory map indicates that there is one read address and 13 write addresses. Output memory map addresses 6-9 are not used and 10-13 are used to specify safe state values that are not used in this example. Therefore, the output memory map words 0-5 correspond to the first six write words specified in the address spreadsheet. See Figure 6-76 for the input memory map and Figure 6-77 for the output memory map for the 1794-OE4/B module.

Input I	Map															
Bit⇒ Word↓	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	P U				I	Not us	ed – s	et to C	)				W 3	W 2	W 1	W 0
Where:	W = volta PU =	Diagn ige ou = Pow	iostic I tputs.) er up I	bits for ) bit	<sup>r</sup> curre	nt out	put wii	e broł	ken or	load r	esista	nce hi	gh. (N	ot use	d on	



Outpu	l Ivia	μ														
Bit⇒ Word↓	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	S						Ana	alog Da	ata – (	Chann	el O					
1	S						Ana	alog Da	ata – (	Chann	el 1					
2	S						Ana	alog Da	ata – (	Chann	el 2					
3	S						Ana	alog Da	ata – (	Chann	el 3					
4					Not	used	– set I	0 0					M 3	M 2	M 1	M 0
5	Not	used	– set t	0 0	C3	C2	C1	C0	Not	used	– set I	0 0	F3	F2	F1	F0
6–9							Not	used	– set l	to 0						
10	S						Safe	state v	alue fo	or cha	nnel 0					
11	S						Safe	state v	alue fo	or cha	nnel 1					
12	S						Safe	state v	alue fo	or cha	nnel 2					
13	S						Safe	state v	alue fo	or cha	nnel 3					
Where:	S = 5 M = C = F = 1	Sign b Multip Config Full ra	it (in 2 lex co jure se nge bi	's com ntrol b elect bi t	ipleme it it	ent)										

Figure 6-77. 1794-OE4/B Module Output Memory Map

Multiplex control bit (M) for individual channels. These bits control the safe state analog outputs. - Bit 00 corresponds to output channel 0, bit 01 corresponds to output channel 1, and so on.

1 = use words 0,1,2 or 3 as directed by channel number n.

0 = use words 10, 11, 12 or 13 as directed by channel number n.

For definition of Fx and Cx bits, see Figure 6-78.

unge Seleette		3						
Channel No.	Ch	<b>. 0</b>	Ch	. 1	Ch	. <b>2</b>	Ch	ı. 3
	F0	C0	F1	C1	F2	C2	F3	C3
Decimal Bits	00	08	01	09	02	10	03	11
0-10V dc/0-20mA	1	0	1	0	1	0	1	0
4–20mA	0	1	0	1	0	1	0	1
-10 to +10V dc	1	1	1	1	1	1	1	1
Off <sup>1</sup>	0	0	0	0	0	0	0	0
C = Configure sel	ect bit							

**Range Selection Bits** 

F = Full range bit

<sup>1</sup> When configured to Off, individual channels will drive 0V/0mA.

Figure 6-78. 1794-OE4/B Write Range Selection Bits

In this example, the read block is set up to monitor the four broken wire bits and the power up bit on the module. The write blocks are set up to configure the module for multiplex control and 0-20mA range. Since all of the multiplex control (M) bits are set to true, the safe state words in addresses 10-13 are not relevant. See Figure 6-79 for example of 1794-OE4/B Read and Write GAP blocks.



Figure 6-79. Example of 1794-OE4/B Read and Write GAP Blocks

### AtlasPC Digital Control, Vol. II (Distributed I/O)

To write the analog output words for the 1794-OE4/B module, CALCULATE blocks were again used. For the 1794-OE4/B module to output the correct current, the GAP block must convert the engineering units requested to raw counts used by the module. The milliamp to raw count relationship can be found in Allen-Bradley manual 1794-6.5.2. See Figure 6-73 for Analog Data Format Table. The table specifies counts in hexadecimal form and the CALCULATE block requires the RAW\_LOW and RAW\_HIGH fields to be entered in decimal form. Under the 0-20mA column, of the Analog Data Format Table, 21mA is equivalent to 7FF8 hexadecimal and 0mA is 0000 hexadecimal. Converting 7FF8 to decimal equals 32760 counts high. In this example, the block scales 0-21mA (engineering units) for 0-32760 counts for the module. The CALCULATE block output is connected to the MODBUS\_M block address associated with the correct memory map address. In this example a 0 to 24 mA tunable set for 4mA is shown for the input to the CALCULATE block. See Figure 6-80 for example of 1794-OE4/B GAP Analog Write Blocks.





An AO requires a limiter on the input value to keep it from exceeding the 21 mA value. Values above 21 mA will roll back over to zero.

NOTICE

## Allen-Bradley Thermocouple Input (1794-IT8) Module



In this example, the first six channels are used for thermocouples and the last two channels are used for monitoring the reference junction temperatures. See Figure 6-81 for example of 1794-IT8 module wiring.





The memory map indicates that there are eleven read addresses and 3 write address. See Figure 6-82 for the input memory map and Figures 6-83 through 6-86 for the output memory map for the 1794-IT8 module.

Thermocoup	ole/m	V Inj	put N	lodu	le (17	94-I	T8) R	ead								
Decimal Bit	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Octal Bit	17	16	15	14	13	12	11	10	07	06	05	04	03	02	01	00
Read Word 0									Reserve	ed						
1								Chan	nel O Inp	out Data	l					
2		Channel 1 Input Data Channel 2 Input Data														
3		Channel 2 Input Data Channel 2 Input Data														
4	Channel 2 Input Data Channel 3 Input Data															
5								Chan	nel 4 Inp	out Data	l					
6								Chan	nel 5 Inp	out Data	l					
7								Chan	nel 6 Inp	out Data	L					
8								Chan	nel 7 Inp	out Data	l					
9				Overra	ange B	its						Under	range B	iits		
10	0	0	0	0	0	Bad Cal	Cal Done	Cal Range	0	Diaç	gnostic S	Status	Pwr Up	Bad Structure	CJC over	CJC Under

Figure 6-82. 1794-IT8 Module Input Memory Map

**Underrange bits**—These bits are set if the input signal is below the input channel's minimum range.

**Overrange bits**—These bits are set if 1), the input signal is above the input channel's maximum range, or 2), an open detector is detected.

**Cold Junction sensor underrange bit**—This bit is set if the cold junction temperature is below 0 °C.

**Cold Junction sensor overrange bit**—This bit is set if the cold junction temperature is above 70 °C.

**Bad Structure**—This bit is set if an invalid thermocouple type is selected. **Powerup bit**—This bit is set (1) until configuration data is received by the module.

**Critical Error bits**—If these bits are anything other than all zeroes, return the module to the factory for repair.

**Calibration Range bit**—Set to 1 if a reference signal is out of range during calibration.

**Calibration Done bit**—Set to 1 after an initiated calibration cycle is complete. **Calibration Bad bit**—Set to 1 if the channel has not had a valid calibration.

Dec. Bit	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Octal Bit	17	16	15	14	13	12	11	10	07	06	05	04	03	02	01	00
Write Word 0	8-Bit Calibration Mask						Cal Clk	Cal hi Cal lo	Filter Cutoff			FDF	Data	Туре		
1	Therr	mocou	ple 3	Туре	Th	ermocou	uple 2 T	уре	Thermocouple 1 Type			/pe	Thermocouple 0 Type			
2	Therr	mocou	ple 7	Туре	Th	Thermocouple 6 Type Thermocouple 5 Type					/pe	Thermocouple 4 Type				
Where: FDF = fixed (	digital filt	ler bit														

Thermocouple/mV Input Module (1794-IT8) Write

Figure 6-83. 1794-IT8 Module Output Memory Map

Word	Decimal Bit (Octal Bit)		Description											
Write Word 0	00-01 (00-01)	Module	e Data T	уре										
		Bit	01	00	Definit	ion								
			0	0 °C (default)										
			0	1										
			1	0	counts scaled between -32768 and +32767									
			1	1	Unipola	ar counts scaled between 0 and 65535								
	Bit 02 (02)	Fixed 1 100% of 100% of 100\% o	Digital F of a Full It – filter	filter – V Scale st r disabl	Vhen this ep input ed.)	s bit is set (1), a software digital filter is enabled. This filter settles to in 60 times the selected first notch filter time shown on page 4–3.								
	03-05 (03-05)	A/D Fil	lter First	t Notch	Frequer	ncy								
		Bit	05	04	03	Definition								
			0	0	0	10Hz (default)								
			0	0	1	25Hz								
			0	1	0	50Hz								
			0	1	1	60Hz								
			1	0	0	100Hz								
			1	0	1	250Hz								
			1	1	0	500Hz								
			1	1	1	1000hZ								
	06 (06)	Calibra	tion High	h/Low bi	t - This I	bit is set during gain calibration; reset during offset calibration.								
	07 (07)	Calibra calibrat	tion cloc tion.	k – this	bit must	be set to 1 to prepare for a calibration cycle; then reset to 0 to initiate								
	08-15 (10-17)	Calibra corresp	tion mas conds to	sk – The channe	Calibration mask - The channel, or channels, to be calibrated will have the correct mask bit set. Bit 8 corresponds to channel 0, bit 9 to channel 1, and so on.									

Figure 6-84. 1794-IT8 Write Word 0

### Hardware First Notch Filter

A/D Filter First Notch Frequency (effective resolution)	10Hz (16-bits)	25Hz (16-bits)	50Hz (16-bits)	60Hz (16-bits)	100Hz (16-bits)	250Hz (13-bits)	500Hz (11-bits)	1000Hz (9-bits)				
Number of channels scanned	System Throughput (in ms and s)											
1	325	145	85	75	55	37	31	28				
2	650	290	170	150	110	74	62	56				
3	975	435	255	225	165	111	93	84				
4	1.3s	580	340	300	220	148	124	112				
5	1.625s	725	425	375	275	185	155	140				
6	1.95s	870	510	450	330	222	186	168				
7	2.275s	1.015s	595	525	385	259	217	196				
8	2.60s <sup>1</sup>	1.16s	680	600	440	296	248	224				
1 Default setting												

Figure 6-85. 1794-IT8 Hardware First Notch Filter

### AtlasPC Digital Control, Vol. II (Distributed I/O)

Word	Decimal Bit (Octal Bit)		Description									
Write Word 2	00-03 (00-03)	Channel	l 0 Ther	mocoup	le Type							
		Bit	03	02	01	00	Thermocouple Type – Range					
			0	0	0	0	Millivolts (default)					
			0	0	0	1	B 300 to 1800°C (572 to 3272°F)					
			0	0	1	0	E -270 to 1000°C (-454 to 1832°F)					
			0	0	1	1	J -210 to 1200°C (-346 to 2192°F)					
			0	1	0	0	K -71 to 1372°C (-95 to 2502°F)					
			0	1	0	1	R -50 to 1768°C (-58 to 3214°F)					
			0	1	1	0	S -50 to 1768°C (-58 to 3214°F)					
			0	1	1	1	T -73 to 400°C (-99 to 752°F)					
			1	0	0	0	C 0 to 2315°C (32 to 4199°F)					
			1	0	0	1	N -270 to 1300°C (-450 to 2372°F)					
			1	0	1	0	Reserved					
			1	0	1	1	Reserved					
			1	1	0	0	Module reports cold junction temperature for channels 00-03					
			1	1	0	1	Module reports cold junction temperature for channels 04-07					
			1	1	1	0	Reserved					
			1	1	1	1	No sensor connected (do not scan)					
	04-07 (04-07)	Channel	l 1 Ther	mocoup	le Type	(see bits	s 00–03)					
	08-11 (10-13)	Channel	2 Ther	mocoup	le Type	(see bits	s 00-03)					
	12-15 (14-17)	Channel	Channel 3 Thermocouple Type (see bits 00–03)									
Write Word 3	00-03 (00-03)	Channel	4 Ther	mocoup	le Type	(see wri	te word 2, bits 00-03)					
	04-07 (04-07)	Channel	l 5 Ther	mocoup	le Type	(see wri	te word 2, bits 00-03)					
	08-11 (10-13)	Channel	i 6 Ther	mocoup	le Type	(see wri	te word 2, bits 00-03)					
	12-15 (14-17)	Channel	l 7 Ther	mocoup	le Type	(see wri	te word 2, bits 00-03)					

Figure 6-86. 1794-IT8 Write Word 1 and 2 (Note: Write Words 2 & 3 should be labeled 1 & 2)

In this example, the first read block is set up to monitor the underrange and overrange bits on the module. The second read block monitors the Cold Junction sensor underrange bit, Cold Junction sensor overrange bit, Bad Structure, Powerup bit, Critical Error bits, Calibration Range bit, Calibration Done bit, and Calibration Bad bit. The first write word (0) sets the module for °F units, 100 Hz filtering, and no calibration. The second write word (1) sets the module for type K thermocouples on channels 0, 1, 2, and 3. The third write word (2) sets the module for type K thermocouples for channels 4 and 5, cold junction (channels 0-3) temperature on channel 6, and cold junction (channels 4-7) on channel 7. See Figure 6-87 for GAP read and write block example.

Manual 85586V2



Figure 6-87. Example of 1794-IT8 Read and Write GAP Blocks

To read the analog input words for the 1794-IT8 module, DIVIDE blocks were used. According to the 1794-IT8 manual, the thermocouple module's output must be scaled to one tenth the value read by the 3170-MBS interface module. See Figure 6-88 for Input scaling of the thermocouples.

Input Type	Range	Scaling	Maximum Resolution						
Millivolt	-76.50 to +76.50mV	-7650 to +7650	10µV						
Туре В	300 to 1800°C	3000 to 18000	0.1°C						
Type E	-270 to 1000°C	2700 to 10000	0.1ºC						
Туре Ј	-210 to 1200°C	-2100 to 12000	0.1ºC						
Туре К	-270 to 1372°C	-2700 to 13720	0.1°C						
Type R	-50 to 1768°C	-500 to 17680	0.1°C						
Type S	-50 to 1768°C	-500 to 17680	0.1ºC						
Туре Т	-270 to 400°C	-2700 to 4000	0.1ºC						
Type N	-270 to 1300°C	-2700 to 13000	0.1°C						
Туре С	0 to 2315°C	0 to 23150	0.1°C						
Туре В	572 to 3272°F	5720 to 32720	0.1ºF						
Type E	-454 to 1832°F	-4540 to 18320	0.1ºF						
Туре Ј	-346 to 2192°F	-3460 to 21920	0.1ºF						
Туре К	-454 to 2502°F	-4540 to 25020	0.1°F						
Type R	-58 to 3214°F	-580 to 32140	0.1ºF						
Type S	-58 to 3214°F	-580 to 32140	0.1ºF						
Туре Т	-454 to 752°F	-4540 to 7520	0.1ºF						
Type N	-450 to 2372°F	-4500 to 23720	0.1ºF						
Туре С	32 to 4199°F	320 to 41990	0.1ºF						
Note: In thermocouple mode, scaled number has an implied decimal point 1 digit from the right. For									

# Input Scaling

Note: In thermocouple mode, scaled number has an implied decimal point 1 digit from the right. For example, if reading is 18000, temperature is 1800.0. In millivolt mode, the implied decimal point is to the left of the last 2 digits. For example, if reading is 2250, actual reading is 22.50mV

Figure 6-88. 1794-IT8 Input Scaling

A divide by 10 block is used to scale the thermocouple outputs. Again, from the 1794-IT8 manual, the range of the cold junction (reference junction) sensor is 0-70 °C. It has been found that the output must be scaled to one hundredth the value output by the 3170-MBS interface module. A divide by 100 block is used to accomplish this. The output of the DIVIDE block will be in engineering units (°F). See Figure 6-89 for example of 1794-IT8 GAP Analog Read Blocks.



Figure 6-89. Example of 1794-IT8 GAP Analog Read Blocks

## Allen-Bradley RTD Input (1794-IR8) Module



See Figure 6-90 for example of 1794-IR8 module wiring.





The memory map indicates that there are eleven read addresses and 3 write address. See Figure 6-91 for the input memory map and Figures 6-92 through 6-95 for the output memory map for the 1794-IR8 module.

<b>RTD Analog Inpu</b>	t Module (1794-IR	3) Read Words
------------------------	-------------------	---------------

	· ·															
Decimal Bit	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Octal Bit	17	16	15	14	13	12	11	10	07	06	05	04	03	02	01	00
Word 0		Reserved														
1		Channel 0 Input Data														
2		Channel 1 Input Data														
3		Channel 2 Input Data														
4		Channel 3 Input Data														
5		Channel 4 Input Data														
6							C	hannel 5 l	nput Da	ata						
7							C	hannel 6 I	nput Da	ata						
8		Channel 7 Input Data														
9	Overrange Bits								Underrange Bits							
10	0	0	0	0	0	Bad Cal	Cal Done	Cal Range	0	Di St	agnostic atus Bits	5	Pwr Up	Reserved	0	0

Figure 6-91. 1794-IR8 Module Input Memory Map

**Underrange bits**—These bits are set if the input signal is below the input channel's minimum range.

**Overrange bits**—These bits are set if 1) the input signal is above the input channel's maximum range, or 2) an open detector is detected.

**Powerup bit**—This bit is set (1) until configuration data is received by the module.

**Critical Error bits**—If these bits are anything other than all zeroes, return the module to the factory for repair.

**Calibration Range bit**—Set to 1 if a reference signal is out of range during calibration

**Calibration Done bit**—Set to 1 after an initiated calibration cycle is complete. **Calibration Bad bit**—Set to 1 if the channel has not had a valid calibration.

iti D Tinuio	TD manog mpar module (1794 mo) while words															
Decimal Bit	15	15 14 13 12 11 10 09 08							07	06	05	04	03	02	01	00
Octal Bit	17	16	15	14	13 12 11 10 07 06 05 04							03	02	01	00	
Word 0	8-bit Calibration Mask								Cal Clk	Cal Hi Cal Lo	Filter Cutoff			Enh MDT		от
1		RTD 3	Туре			RTD	2 Туре		RTD 1 Type RTD 0 Type							
2	RTD 7 Type RTD 6 Type								RTD 5 Type RTD 4 Type					уре		
Where: Enh MD	Where: Enh = Enhanced MDT = Module Data Type															

RTD Analog Input Module (1794-IR8) Write Words

Figure 6-92. 1794-IR8 Module Output Memory Map

## AtlasPC Digital Control, Vol. II (Distributed I/O)

Word	Dec. Bits (Octal Bits)					Description														
Write word 0	00-01	Modul	e Data T	уре																
		Bit	01	00																
			0	0	°C (default)															
			0	1 <sup>o</sup> F																
			1	0	0 Bipolar counts scaled between -32768 and +32767															
			1 1 Unipolar counts scaled between 0 and 65535																	
	02	Enhan compa reduce	thanced mode select – measures voltage drop across a precision resistor in the module to impare with the unknown input. This improves module temperature drift characteristics, but duces module throughput.																	
	03-05	A/D Fil	√D Filter First Notch Frequency																	
		Bit	05	04	Definition															
				0	0	0	10Hz (default)													
									ĺ								0	0	1	25Hz
				0	1	0	50Hz													
			0	1	1	60Hz														
			1	1	0	0	100Hz													
			1	0	1	250Hz														
			1	1	0	500Hz														
			1000Hz																	
	06	Calibra	ation Hig	gh/Low	bit - Thi	is bit is set during gain calibration; reset during offset calibration.														
	07	Calibra initiate	Calibration clock – this bit must be set to 1 to prepare for a calibration cycle; then reset to 0 to initiate calibration.																	
	08-15 (10-17)	Calibration mask - The channel, or channels, to be calibrated will have the correct mask bit set. Bit 8 corresponds to channel 0, bit 9 to channel 1, and so on.																		

Figure 6-93. 1794-IR8 Write Word 0

#### Hardware First Notch Filter

A/D Filter First Notch Frequency (effective resolution)	10Hz (16-bits)	25Hz (16-bits)	50Hz (16-bits)	60Hz (16-bits)	100Hz (16-bits)	250Hz (13-bits)	500Hz (11-bits)	1000Hz (9-bits)				
Number of channels scanned	System Throughput (in ms and s)											
1	325	145	85	75	55	37	31	28				
2	650	290	170	150	110	74	62	56				
3	975	435	255	225	165	111	93	84				
4	1.3s	580	340	300	220	148	124	112				
5	1.625s	725	425	375	275	185	155	140				
6	1.95s	870	510	450	330	222	186	168				
7	2.275s	1.015s	595	525	385	259	217	196				
8	2.60s <sup>1</sup>	1.16s	680	600	440	296	248	224				
1 Default setting		•				-						

Figure 6-94. 1794-IT8 Hardware First Notch Filter

Word	Dec. Bits (Octal Bits)		Description							
Write Word 1	00-03	Chann	el 0 RTD	Туре						
		Bit	03	02	01	00	RTD Type – Range			
			0	Resistance (default)						
			0	0	0	1	No sensor connected – do not scan			
			0	0	1	0	100 ohm Pt $\alpha$ = 0.00385 Euro (–200 to +870°C)			
			0	0	1	1	100 ohm Pt $\alpha$ = 0.003916 U.S. (–200 to +630°C)			
			0	1	0	0	200 ohm Pt $\alpha$ = 0.00385 Euro (–200 to +630°C)			
			0	1	0	1	500 ohm Pt $\alpha$ = 0.00385 Euro (-200 to +630°C)			
			0	1	1	0	Reserved			
			0	1	1	1	10 ohm Copper (-200 to +260°C)			
			1	0	0	0	120 ohm Nickel (-60 to +250°C)			
			1	0	0	1	100 ohm Nickel (-60 to +250°C)			
			1	0	1	0	200 ohm Nickel (-60 to +250°C)			
			1	0	1	1	500 ohm Nickel (-60 to +250°C)			
			1	1	0	0	Reserved			
			1101 to	o 1111 -	Reserve	ed				
	04-07	Chann	el 1 RTD	) Type (s	see bits	00-03)				
	08-11	Chann	el 2 RTD	) Type (s	see bits	00-03)				
	12-15	Chann								
Write Word 2	00-03	Chann	el 4 RTD	Type (s	see write	word 1,	bits 00-03)			
	04-07	Chann	el 5 RTD	) Type (s	see write	word 1,	bits 00-03)			
	08-11	Chann	el 6 RTD	) Type (s	see write	word 1,	bits 00-03)			
	12-15	Chann	el 7 RTD	) Type (s	see write	word 1,	bits 00-03)			

Figure 6-95. 1794-IT8 Write Word 1 and 2

In this example, the first read block is set up to monitor the underrange and overrange bits on the module. The second read block monitors the Powerup bit, Critical Error bits, Calibration Range bit, Calibration Done bit, and Calibration Bad bit. The first write word (0) sets the module for °F units, 100 Hz filtering, and no calibration. The second write word (1) sets the module for 100 ohm Pt Euro RTD on channels 0, 1, 2, and 3. The third write word (2) sets the module for 100 ohm Pt Euro RTD for channels 4, 5, 6, and 7. See Figure 6-96 for GAP read and write block example.

#### AtlasPC Digital Control, Vol. II (Distributed I/O)



Figure 6-96. Example of 1794-IR8 Read and Write GAP Blocks

To read the analog input words for the 1794-IR8 module, DIVIDE blocks were used. According to the 1794-IR8 manual, the RTD module's output must be scaled to one tenth the value read by the 3170-MBS interface module. From the 1794-IR8 Input Scaling, it can be seen that the 100 ohm Pt Euro RTD range is – 328 to 1598 °F. The output of the DIVIDE block will be in engineering units (°F). See Figure 6-97 for Input scaling for RTDs.

Range	Degrees	Counts	Maximum Resolution
100 ohm Pt Euro	-328 to +1598°F	-3280 to +15980	0.1ºF
100 ohm Pt U.S	-328 to +1166°F	-3280 to +11660	0.1ºF
200 ohm Pt Euro	-328 to +1166°F	-3280 to +11660	0.1ºF
500 ohm Pt Euro	-328 to +1166°F	-3280 to +11660	0.1ºF
100 ohm Nickel	-76 to +482°F	-760 to +4820	0.1ºF
120 ohm Nickel	-112 to +500°F	-1120 to +5000	0.1°F
200 ohm Nickel	-76 to +482°F	-760 to +4820	0.1°F
500 ohm Nickel	-76 to +482°F	-760 to +4820	0.1°F
10 ohm Copper	-328 to +500°F	-3280 to +5000	0.1°F
Note: Temperature data has an implied	d decimal point 1 space to the right	of the last digit. (divide by 10). For	example, a

#### Input Scaling

Note: Temperature data has an implied decimal point 1 space to the right of the last digit. (divide by 10). For example, a readout of 1779° would actually be 177.9°.

Figure 6-97. 1794-IR8 Input Scaling

See Figure 6-98 for example of 1794-IR8 GAP Analog Read Blocks.



Figure 6-98. Example of 1794-IR8 GAP Analog Read Blocks

# Automation Direct Terminator I/O Example

## Automation Direct Terminator I/O Modbus Configuration

MODBUS is an application layer messaging protocol, at level  $\overline{7}$ , as defined in the OSI (Open System Interconnection) model. It provides client/server communication between devices connected on different types of buses or networks. It is a request/reply protocol and offers services specified by function codes. MODBUS function codes are elements of MODBUS request/reply PDUs (Protocol Data Unit).

Modicon developed the Modbus addressing scheme around the data table and I/O structure in Modicon PLCs. Terminator I/O is a modular system which combines the functions of terminal blocks and I/O modules for distributed I/O. Each Terminator I/O system has the following components: a Power Supply, a Base Controller, and one or more I/O Module(s). Terminator I/O systems can contain up to 16 I/O modules per slave (node). Each slave (node) system can be divided into one row of base I/O plus two rows of local expansion I/O using a base expansion cable.

In this example, one T1K-MODBUS adapter and two power supplies from Automation Direct are interfaced with seven terminal base units with installed Terminator I/O modules, forming a Terminator I/O system.

The T1K-MODBUS is a Network Interface Adapter that communicates between the Terminator I/O modules backplane and the AtlasPC/Master across a serial RS-232 connection. The T1K-MODBUS module is a slave device to the AtlasPC control, and is a master controller of the Terminator I/O modules. The I/O data exchange occurs as follows. Output data is sent from the AtlasPC control across the RS-232 connection to the T1K-MODBUS adapter. The network interface adapter then automatically transfers the data across the Terminator I/O backplane to the output modules. Inputs from the input modules are collected by the network interface adapter via the backplane and sent across the RS-232 connection to the AtlasPC control.

### AtlasPC Digital Control, Vol. II (Distributed I/O)

In order to simplify the nomenclature used in creating the GAP application, certain naming conventions were changed with respect to the manufacturer's naming convention. In this example, Woodward refers to the node address as the Group address. The T1K-MODBUS Group address, (Node address), is set by two rotary switches located on the front of the T1K-MODBUS module. In this example the address is set to 01.

The Automation Direct Terminator I/O system requires DIN rail mounted power supplies to power the individual I/O module over the Terminator I/O back plane. In this example, a 120 Vac unit (T1K\_01AC) was used to power the Discrete I/O modules and a 24 Vdc unit (T1K-01DC was used to power the Analog I/O modules.

In this example, the power supplies were also used to generate the needed current for the external power requirements of the circuits. See Figure 6-99 for Automation Direct Terminator I/O configuration layout.



Figure 6-99. Automation Direct Terminator I/O Configuration

### Address Spreadsheet

The I/O map for a module is divided into read words and write words. Read words consist of input and status words, and write words consist of output and configuration words. The number of read words or write words can be 0 or more.

To keep track of the addressing for all of the reads and writes, an address spreadsheet is very useful. This address spreadsheet can be derived from memory maps in the I/O modules User Manual and the network interface module (head) T1K-MODBUS User Manual. These memory maps define which addresses to allocate within the Address Spreadsheet. Not all of the addresses allocated to each module are written to or read from. Some addresses are either not used or reserved. See specific I/O module memory maps for detail functionality used to define the GAP reads and writes. The Automation Direct Terminator I/O system addresses its discrete I/O by bits and analog I/O by words. See Table 6-6 for the address spreadsheet for this example.

Module	Byte #	Read Address Bits	Write Address Bits
T1K-MODBUS	0	None	None
T1K-08ND3	0	10000-10008	None
T1K-16ND3	0	10009-10016	None
	1	10017-10024	None
T1K-16TD1	0	None	00000-00008
	1	None	00009-00016
T1K-08TRS	0	None	00017-00024
Module	Word #	Read Addr. Words	Write Addr. Words
T1F-16AD-1	0	30001	None
	1	30002	
	2	30003	
	3	30004	
	29	30030	
	30	30031	
	31	30032	
T1F-16DA-1	0	None	40001
	1		40002
	2		40003
	3		40004
	29		40030
	30		40031
	31		40032
T1F-14THM	0	30033	None
	1	30034	
	2	30035	
	3	30036	
	29	30062	
	30	30063	
	31	30064	

Table 6-6. Modbus Word Address Spreadsheet

Use the following documents from the manufacturer to obtain the Memory Maps and related information.

Module Document P/N I/O modules T1K-INST-M Modbus Interface T1K-MODBUS-M

#### Nomenclature

When creating a new GAP application, it is important to establish a well organized block naming convention up front. Once done, it is easier to find specific functions and I/O within a large GAP application. Though not shown in this example, the Category and Block Names could follow similar nomenclature rules to those shown in Chapter 1 (Profibus).

#### GAP Application

In order to communicate between the Atlas serial RS-232 port and the T1K-MODBUS, a MOD\_PORT and MODBUS\_M block must be defined in GAP. The MOD\_PORT block defines the serial communications baud rate, stop, parity, and type of interface (RS-232, 422, 485). The MODBUS\_M block defines the addressing for Modbus communications between the Atlas and the distributed I/O. Based on the Address Spreadsheet, this block can be customized to read and write to appropriate addresses. See Figure 6-100 for MODBUS\_M/MOD\_PORT setup example.

			A02_MAIN
]	A02_MAIN		MODBUS2
	COMM_02	A02_MAIN.COMM_02.MOD_PORT-	PORT_1
10 (1, 12)-	BAUD		E_ERR_1_1
	MOD_PORT		M_RST
*1 (1, 3)-	STOP		L_ERR_1_1
	P_STATUS	*FALSE-	I_MOD_1
*1 (1, 3)-	PARITY		E_NUM_1_1
	FAULT	*FALSE-	E_RST_1
*1 (1, 3)-	DRIVER		
[	MOD_PORT	*2 (1, 2)-	ASCII_RTU
			MODBUS M 5

Figure 6-100. MODBUS\_M Block Example

The E\_ERR\_1\_x output field on the MODBUS\_M block is used to display Exception Error on PORT\_1 per RPTx. It latches TRUE when an exception error is detected. E\_NUM\_1\_X (hidden) displays the error number. See Table 6-7 for exception errors.

CODE	NAME	MEANING							
The fo	The following are generated by the slave.								
00	NO ERROR	Error free							
01	ILLEGAL FUNCTION	Message function received is not an allowable action for addressed slave. (Unsupported or illegal function code).							
02	ILLEGAL DATA ADDRESS	Address referenced in data field is not an allowable address for the addressed slave location. (Master requested data which is not configured from slave).							
03	ILLEGAL DATA mount of data requested from slave was too large for slave to value   VALUEA return in a single response.								
The fo	llowing are generat	ed by the master.							
09	CHECKSUM ERROR	Error in checksum in message from slave. Can indicate link quality and/or noise problems.							
10	GARBLED MESSAGE	Data received from the slave, but is too short to be a valid Modbus message/response.							
20	UNSOLICITED RESPONSE	Unsolicited message received from slave.							
21	BAD FC IN RESPONSE	Slave returned a message with a different function code from the command sent.							
22	BAD ADD IN RESPONSE	Slave returned a message with a different address from the command sent.							
23	NO SLAVE RESPONSE	No response from slave.							
24	MOE/CODER ERROR	MOE/CODER error.							
25	INTERNAL SYS ERROR	Internal system error.							

Table 6-7. MODBUS\_M Exception Errors

The L\_ERR\_1\_x is used to display Link Error on PORT\_1 for RPTx. It goes TRUE when the slave fails to answer a data request. If a response isn't received in TIME\_OUT\_x seconds, the request is retried. If a response isn't received in TIME\_OUT\_x seconds after the request is retried, then this output is set true.

While waiting for a response from one slave, the master is not communicating with the other slaves. So, if multiple slaves fail at the same time (i.e. broken cable), the L\_ERR\_1\_x for the first slave attempted will occur at 2 x TIME\_OUT\_x. But, the second L\_ERR\_1\_x won't go true until 2 x TIME\_OUT\_x after the first failure because no communications are attempted with that slave until after the first has timed out.

In this example, the TIK-MODBUS adapter is configured for the 584 / 984 Addressing mode (Dip switch 7). See Figure 6-101 for the full T1K-MODBUS adapter addressing table.

Mo	dbus Turne	T1K-MODBUS						
Dat	атуре	Range (Decimal)	Poi	nts	Memory Type			
	Coll	1 – 1024	1024		Discrete Output			
	2011	1025 – 9999	-		not supported			
	amut	10001 – 11024	1024		Discrete Input			
	iput	11025 – 19999	-		not supported			
Madhur	Data Tura		V Memo	ry Range				
Modbus	bata Type	Range (Decimal)	Words (16– bit)	Channel (32– bit)	Memory Type			
	Analog Input	30001 - 30128	128 64		Analog Input Register			
	Input Register	30129 - 38999	-	-	not supported			
Input Register	Bit Input Register	30201 - 30264	64	-	Discrete Input Bit Register			
	Input Register	39129 - 39999	-	-	not supported			
	Analog output	40001 – 40128	128	64	Analog Output Register			
	Hold Register	40129 - 40200	-	-	not supported			
Hold Register	Bit Output Register	40201 – 40264	64		Discrete Output Bit Register			
	Hold Register	40265 - 49000	-	-	not supported			
	Hold Register	49001 - 49128	128	-	Special Register			
	Hold Register	49129 - 49999	-	-	not supported			

Figure 6-101. T1K-MODBUS Adapter Addressing Table

In the RPT window for the MODBUS\_M block, the BR\_F\_CODE and AR\_F\_CODE fields specify the Boolean and Analog read Function Codes for Modbus. The Boolean Read Function Code input defines the Boolean read and write addresses as follows:

1 = 00001-0FFFF Input Coils (Boolean READ/WRITE) 2 = 10001-1FFFF Input Status (Boolean READ ONLY)

The Analog Read Function Code input defines the Analog read and write addresses as follows:

3 = 40001-4FFFF Holding Registers (Analog READ/WRITE)

4 = 30001-3FFFF Input Registers (Analog READ ONLY)

By setting the BR\_F\_CODE to 2 and the AR\_F\_CODE field to 4 (defaults), the MODBUS\_M block will access the following addresses as specified by the 584 / 984 Addressing mode of the T1K-MODBUS adapter:

1 – 1024 Discrete Outputs 10001 – 11024 Discrete Inputs 30001 – 30128 Analog Input Registers 30201 – 30264 Bit Input Registers 40001 – 40128 Analog Output Registers 40201 – 40264 Bit Output Registers

The S\_ADD\_1 field must agree with the Group or Node address for the T1K-MODBUS adapter. In this example, the address is set to 01 which matches the two rotary switch settings on the adapter. See Figure 6-102 for example of MODBUS\_M repeat fields.

_			
	hide	< S_ADD_1	1
	hide	< S_IP_1_1	(0)
	hide	< S_IP_2_1	(0)
	hide	< S_IP_3_1	(0)
	hide	< S_IP_4_1	(0)
	hide	< S_PORT_1	(0)
	show	< I_MOD_1	*FALSE
	show	< E_RST_1	*FALSE
	hide	< TIMEOUT_1	(1.5)
	show	> E_NUM_1_1	
	show	> E_ERR_1_1	
	show	> L_ERR_1_1	
	hide	> E_NUM_2_1	
	hide	> E_ERR_2_1	
	hide	> L_ERR_2_1	
	hide	< BW_ADD_1	0
	>>	RPTbw1	
	hide	< BR_F_CODE_1	(2)
	hide	< BR_ADD_1	0
	>>	RPTbr1	
	hide	< AR_F_CODE_1	(4)
	hide	< AR_ADD_1	
	>>	RPTar1	
	hide	< AW_ADD_1	0
1	>>	RPTaw1	
			,

Figure 6-102. MODBUS\_M Block RPT Example

Within the MODBUS\_M RPT window, there are four repeats (RPTbw1, RPTbr1, RPTar1, and RPTaw1). Each one of these RPT fields opens another window which displays the addresses assigned for that particular RPT. See specific module sections below for memory map function assignment. Example for the T1K-08ND3 module bits (BR\_V\_1\_1): since the starting address is 10000, the BR\_F\_CODE = 2. The BR\_ADD\_1 offset is 0. Therefore the T1K-08ND3 module bit (BR\_V\_1\_1) has an address of 10000 + 0 + 1 = 10001. All of the addresses specified in the address spreadsheet are mapped into the MODBUS\_M block by applying this formula. See Figures 6-103, 6-104, 6-105, and 6-106 for all read/write address windows. Figure 6-107 shows the write addresses for the discrete output modules (T1K-16TD1 and T1K-08TRS), addresses 00001 to 00024.

hide < BY	V_C_1_1	16TD1 CH1	hide	< BW_C_1_13	16TD1 CH13
hide < BY	V V 1 1	AD16TD1.BO_01.B_NAME	hide	< BW_V_1_13	AD16TD1.BO_13.B_NAME
hide < BY	V_C_1_2	16TD1 CH2	hide	< BW_C_1_14	16TD1 CH14
hide < BY	V V 1 2	AD16TD1.BO 02.B NAME	hide	< BW_V_1_14	AD16TD1.BO_14.B_NAME
hide < BY	V C 1 3	16TD1 CH3	hide	< BW_C_1_15	16TD1 CH15
hide < BY	v v 1 3	AD16TD1.BO 03.B NAME	hide	< BW_V_1_15	AD16TD1.BO_15.B_NAME
hide < BY	V C 1 4	16TD1 CH4	hide	< BW_C_1_16	16TD1 CH16
hide < BY	v v 1 4	AD16TD1.BO 04.B NAME	hide	< BW_V_1_16	AD16TD1.BO_16.B_NAME
hide < BY	V C 1 5	16TD1 CH5	hide	< BW_C_1_17	08TRS CH1
hide < BY	V V 1 5	AD16TD1.BO 05.B NAME	hide	< BW_V_1_17	AD08TRS.BO_1.B_NAME
hide < BY	V C 1 6	16TD1 CH6	hide	< BW_C_1_18	08TRS CH2
hide < BY	V V 1 6	AD16TD1.BO 06.B NAME	hide	< BW_V_1_18	AD08TRS.BO_2.B_NAME
hide < BY	Y C 1 7	16TD1 CH7	hide	< BW_C_1_19	08TRS CH3
hide < BY	V V 1 7	AD16TD1.BO 07.B NAME	hide	< BW_V_1_19	AD08TRS.BO_3.B_NAME
hide < BY	Y C 1 8	16TD1 CH8	hide	< BW_C_1_20	08TRS CH4
hide < BY	V V 1 8	AD16TD1.BO 08.B NAME	hide	< BW_V_1_20	AD08TRS.BO_4.B_NAME
hide < BY	V C 1 9	16TD1 CH9	hide	< BW_C_1_21	08TRS CH5
hide < BY	V V 1 9	AD16TD1.BO 09.B NAME	hide	< BW_V_1_21	AD08TRS.BO_5.B_NAME
hide < BY	V C 1 10	16TD1 CH10	hide	< BW_C_1_22	08TRS CH6
hide < BY	V V 1 10	AD16TD1.BO 10.B NAME	hide	< BW_V_1_22	AD08TRS.BO_6.B_NAME
hide < BY	V C 1 11	16TD1 CH11	hide	< BW_C_1_23	08TRS CH7
hide < BY	V V 1 11	AD16TD1.BO 11.B NAME	hide	< BW_V_1_23	AD08TRS.BO_7.B_NAME
hide < BY	Y C 1 12	16TD1 CH12	hide	< BW_C_1_24	08TRS CH8
hide < BY	V_V_1_12	AD16TD1.B0_12.B_NAME	hide	< BW_V_1_24 👻	AD08TRS.BO_8.B_NAME

Figure 6-103. MODBUS\_M Block Boolean Write RPT Example

Figure 6-104 shows all of the used read input addresses for Discrete Input
modules (T1K-08ND3 and T1K-16ND3), addresses 10001 to 10024.

hide	< BR C 1 1	08ND3 CH1	hide	< BR_C_1_9	16ND3 CH1	hide	< BR_C_1_17	16ND3 CH9
hide	> BR V 1 1		hide	> BR_V_1_9		hide	> BR_V_1_17	
hide	< BR D 1 1	(FALSE)	hide	< BR_D_1_9	(FALSE)	hide	< BR_D_1_17	(FALSE)
hide	< BR C 1 2	08ND3 CH2	hide	< BR_C_1_10	16ND3 CH2	hide	< BR_C_1_18	16ND3 CH10
hide	> BR V 1 2		hide	> BR_V_1_10		hide	> BR_V_1_18	
hide	< BR D 1 2	(FALSE)	hide	< BR_D_1_10	(FALSE)	hide	< BR_D_1_18	(FALSE)
hide	< BR C 1 3	08ND3 CH3	hide	< BR_C_1_11	16ND3 CH3	hide	< BR_C_1_19	16ND3 CH11
hide	> BR V 1 3		hide	> BR_V_1_11		hide	> BR_V_1_19	
hide	< BR D 1 3	(FALSE)	hide	< BR_D_1_11	(FALSE)	hide	< BR_D_1_19	(FALSE)
hide	< BR C 1 4	08ND3 CH4	hide	< BR_C_1_12	16ND3 CH4	hide	< BR_C_1_20	16ND3 CH12
hide	> BR V 1 4		hide	> BR_V_1_12		hide	> BR_V_1_20	
hide	< BR D 1 4	(FALSE)	hide	< BR_D_1_12	(FALSE)	hide	< BR_D_1_20	(FALSE)
hide	< BR C 1 5	08ND3 CH5	hide	< BR_C_1_13	16ND3 CH5	hide	< BR_C_1_21	16ND3 CH13
hide	> BR_V_1_5		hide	> BR_V_1_13		hide	> BR_V_1_21	
hide	< BR D 1 5	(FALSE)	hide	< BR_D_1_13	(FALSE)	hide	< BR_D_1_21	(FALSE)
hide	< BR C 1 6	08ND3 CH6	hide	< BR_C_1_14	16ND3 CH6	hide	< BR_C_1_22	16ND3 CH14
hide	> BR V 1 6		hide	> BR_V_1_14 🚽		hide	> BR_V_1_22	
hide	< BR_D_1_6	(FALSE)	hide	< BR_D_1_14	(FALSE)	hide	< BR_D_1_22	(FALSE)
hide	< BR_C_1_7	08ND3 CH7	hide	< BR_C_1_15	16ND3 CH7	hide	< BR_C_1_23	16ND3 CH15
hide	> BR_V_1_7		hide	> BR_V_1_15		hide	> BR_V_1_23	
hide	< BR_D_1_7	(FALSE)	hide	< BR_D_1_15	(FALSE)	hide	< BR_D_1_23	(FALSE)
hide	< BR_C_1_8	08ND3 CH8	hide	< BR_C_1_16	16ND3 CH8	hide	< BR_C_1_24	16ND3 CH16
hide	> BR_V_1_8	l l	hide	> BR_V_1_16		hide	> BR_V_1_24	
hide	< BR_D_1_8	(FALSE)	hide	< BR_D_1_16	(FALSE)	hide	< BR_D_1_24 👻	(FALSE)

Figure 6-104. MODBUS\_M Block Boolean Read RPT Example

Figure 6-105 shows all of the used read input addresses for analog Input modules (T1F-16AD-1 and T1F-14THM), addresses 30001 to 30060.

**IMPORTANT** The Automation Direct analog modules use two address words per channel. The first word is used, and the second is not used. The unused address must be accounted for when addressing the modules and therefore requires each channel to increment by two

modules and therefore requires each channel to increment by two addresses. Example: 2X16 addresses for the T1F-AD-1 module + 2X14 addresses for the T1F-14THM module = 60 addresses total.

hide < AR C 1 1	16AD-1 CH1	hide < AR_C_1_11	16AD-1 CH6	hide < AR_C_1_21	16AD-1 CH11	hide < AR_C_1_31	16AD-1 CH16	hide < AR_C_1_41	14THM CH5	hide < AR_C_1_51	14THM CH10
hide > AR V 1 1		hide > AR_V_1_11		hide > AR_V_1_21		hide > AR_V_1_31		hide > AR_V_1_41		hide > AR_V_1_51	
hide KAR M 1 1	1.0	hide < AR_M_1_11	(1.0)	hide < AR_M_1_21	(1.0)	hide < AR_M_1_31	(1.0)	hide < AR_M_1_41	(1.0)	hide < AR_M_1_51	(1.0)
hide < AR D 1 1	lio.oi	hide < AR_D_1_11	(0.0)	hide < AR_D_1_21	(0.0)	hide < AR_D_1_31	(0.0)	hide < AR_D_1_41	(0.0)	hide < AR_D_1_51	(0.0)
hide < AB C 1 2		hide < AR_C_1_12		hide < AR_C_1_22		hide < AR C 1 32		hide < AR C 1 42	· ·	hide < AR_C_1_52	
hide > AB V 1.2		hide > AR_V_1_12		hide > AR_V_1_22		hide > AR V 1 32		hide > AR V 1 42		hide > AR_V_1_52	
hide < AB M 1.2	1.0	hide < AR_M_1_12	(1.0)	hide < AR_M_1_22	(1.0)	hide < AR M 1 32	[1.0]	hide < AR M 1 42	(1.0)	hide < AR_M_1_52	(1.0)
hide (AB D 1 2		hide < AR_D_1_12	(0.0)	hide < AR_D_1_22	(0.0)	hide < AR D 1 32	(0.0)	hide < AR D 1 42	n.on	hide < AR D 1 52	(0.0)
hide CAB C 1 3	164D-1 CH2	hide < AR_C_1_13	16AD-1 CH7	hide < AR_C_1_23	16AD-1 CH12	hide < AR C 1 33	14THM CH1	hide < AR C 1 43	14THM CH6	hide < AR C 1 53	14THM CH11
hide AB V 1 3	TOND TONE	hide > AR_V_1_13		hide $> AR_V_1_23$		hide > AR V 1 33		hide > AR V 1 43		hide > AR V 1 53	
hide CAB M 1 3	n n	hide < AR_M_1_13	(1.0)	hide < AR_M_1_23	(1.0)	hide < AR M 1 33	r1.01	hide < AR M 1 43	r1.01	hide < AR M 1 53	(1.0)
hide CAB D 1 3	0.0	hide < AR_D_1_13	(0.0)	hide < AR_D_1_23	(0.0)	hide < AR D 1 33	io.oi	hide < AR D 1 43	10.01	hide < AR D 1 53	(0.0)
hide CAB C 1 4	(0.0)	hide < AR_C_1_14	II	hide < AR_C_1_24		hide < AR C 1 34	l í	hide < AR C 1 44	(=:=)	hide < AR C 1 54	
		hide > AR V 1 14 -	1	hide > AR V 1 24	1	hide > AB V 1 34		hide > AB V 1 44		hide > AR V 1 54	
	n n	hide < AR M 1 14	(1.0)	hide < AR M 1 24	(1.0)	hide (AB M 1 34	r1.01	hide CAB M 1 44	r1.01	hide < AR M 1 54	n.0
	(1.0)	hide < AR D 1 14	0.0	hide < AR D 1 24	10.0	hide (AR D 1 34	(0.0)	hide (AB D 1 44	0.0	hide < AR D 1 54	n.oi
	16AD-1 CH3	hide < AR C 1 15	16AD-1 CH8	hide < AR C 1 25	16AD-1 CH13	hide (AB C 1 35	14THM CH2	hide CAB C 1 45	14THM CH7	hide < AR C 1 55	14THM CH12
	TOND I CITS	hide > AR V 1 15		hide > AR V 1 25		hide > AB V 1 35		hide > AB V 1 45		hide > AR V 1 55	
hide (AD M 1.5	n m	hide < AR M 1 15	(1.0)	hide < AR M 1 25	(1.0)	hide (AB M 1 35	r1.01	hide (AB M 1 45	r1.01	hide < AR M 1 55	n.0
	(1.0)	hide < AR D 1 15	0.0	hide < AR D 1 25	0.0	hide (AR D 1 35	(0.0)	hide (AB D 1 45	0.0	hide < AR D 1 55	10.01
hide (AP C 1 6	(010)	hide < AR C 1 16		hide < AR C 1 26	- I	hide < AB C 1 36		hide < AB C 1 46	(,	hide < AR C 1 56	
hide AB V 1.6		hide > AR_V_1_16		hide > AR_V_1_26		hide > AR V 1 36		hide > AR V 1 46		hide > AR V 1 56	
hide ( AP M 1.6	r1 m	hide < AR M 1 16	(1.0)	hide < AR M 1 26	(1.0)	hide < AB M 1 36	1.0	hide < AB M 1 46	r1.m	hide < AR M 1 56	n.0
hide CAB D 1.6	0.0	hide < AR_D_1_16	(0.0)	hide < AR_D_1_26	(0.0)	hide < AR D 1 36	0.0	hide < AR D 1 46	10.01	hide < AR D 1 56	0.0
hide (AP C 1 7	16AD-1 CH4	hide < AR C 1 17	16AD-1 CH9	hide < AR C 1 27	16AD-1 CH14	hide < AB C 1 37	14THM CH3	hide < AB C 1 47	14THM CH8	hide < AR C 1 57	14THM CH13
hide AB V 1 7		hide > AR_V_1_17		hide > $AR_V_1_27$		hide > AR V 1 37		hide > AR V 1 47		hide > AR V 1 57	
hide CAB M 1.7	n m	hide < AR_M_1_17	(1.0)	hide < AR_M_1_27	(1.0)	hide < AR M 1 37	n.0	hide < AR M 1 47	. 11.01	hide < AR M 1 57	r1.01
hide CAB D 1 7	0.0	hide < AR_D_1_17	(0.0)	hide < AR_D_1_27	(0.0)	hide < AR D 1 37	0.0	hide < AR D 1 47	10.01	hide < AR D 1 57	io.oj
hide CAB C 1 8	(010)	hide < AR_C_1_18		hide < AR_C_1_28	1 · ·	hide < AR C 1 38	l í	hide < AR C 1 48	(=:=;	hide < AR C 1 58	l í
hide AB V 1.8		hide > AR_V_1_18		hide > AR_V_1_28		hide > AR V 1 38		hide > AR V 1 48		hide > AR V 1 58	
hide CAB M 1.8	n m	hide < AR_M_1_18	(1.0)	hide < AR_M_1_28	[1.0]	hide < AR M 1 38	r1.01	hide < AR M 1 48	11.01	hide < AR M 1 58	r1.01
hide CAB D 1 8	0.0	hide < AR_D_1_18	(0.0)	hide < AR_D_1_28	[0.0]	hide < AR D 1 38	io.oi	hide < AR D 1 48	10.01	hide < AR D 1 58	10.0
hide CAB C 1 9	164D-1 CH5	hide < AR_C_1_19	16AD-1 CH10	hide < AR_C_1_29	16AD-1 CH15	hide < AR C 1 39	14THM CH4	hide < AR C 1 49	14THM CH9	hide < AR C 1 59	1 14THM CH14
hide AB V 1 9		hide > AR_V_1_19		hide > AR_V_1_29		hide > AR V 1 39		hide > AR V 1 49		hide > AR V 1 59	
hide CAB M 1.9	n m	hide < AR_M_1_19	[1.0]	hide < AR_M_1_29	[1.0]	hide < AR M 1 39	r1.01	hide < AR M 1 49	n.0	hide < AR M 1 59	n.n
hide CAB D 1 9	0.0	hide < AR_D_1_19	(0.0)	hide < AR D 1 29	[0.0]	hide < AR D 1 39	io.oi	hide < AR D 1 49	10.01	hide < AR D 1 59	lio.oi
hide CAB C 1 10	,	hide < AR_C_1_20		hide < AR_C_1_30		hide < AR C 1 40		hide < AR C 1 50		hide < AR C 1 60	
hide > AB V 1 10		hide > AR_V_1_20		hide $> AR_V_1_30$		hide > AR V 1 40		hide > AR V 1 50		hide > AR V 1 60	
hide CAB M 1 10	(1.0)	hide < AR_M_1_20	(1.0)	hide < AR_M_1_30	(1.0)	hide < AR M 1 40	[1.0]	hide < AR M 1 50	(1.0)	hide < AR M 1 60	[[1.0]
hide (AB D 1 10	10.01	hide < AR_D_1_20	(0.0)	hide < AR_D_1_30	(0.0)	hide < AR D 1 40	[0.0]	hide < AR D 1 50	(0.0)	hide < AR D 1 60	[[0.0]

Figure 6-105. MODBUS\_M Block Analog Read RPT Example

Figure 6-106 shows all of the used write output addresses for the analog output module (T1F-16DA-1), addresses 40001 to 40032.

Note: The Automation Direct analog modules use two address words per channel. The first word is used, and the second is not used. The un-used address must be accounted for when addressing the modules and therefore requires each channel to increment by two addresses.

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hide	< AW_C_1_1	16DA-1 CH1	hide	< AW_C_1_13	16DA-1 CH7	hide	< AW_C_1_25	16DA-1 CH13
hide	< AW_V_1_1	AD16DA-1.AO_01.CURVE_2D	hide	< AW_V_1_13	AD16DA-1.AO_07.CURVE_2D	hide	< AW_V_1_25	AD16DA-1.AO_13.CURVE_2D
hide	< AW_M_1_1	(1.0)	hide	< AW_M_1_13	(1.0)	hide	< AW_M_1_25	(1.0)
hide	< AW_C_1_2	16DA-1 MODULE CONTROL BYTE	hide	< AW_C_1_14		hide	< AW_C_1_26	
hide	< AW_V_1_2	AD16DA-1.MODCTLBYTE.OUT_1	hide	< AW_V_1_14		hide	< AW_V_1_26	
hide	< AW M 1 2	[1.0]	hide	< AW_M_1_14	(1.0)	hide	< AW_M_1_26	(1.0)
hide	< AW_C_1_3	16DA-1 CH2	hide	< AW_C_1_15	16DA-1 CH8	hide	< AW_C_1_27	16DA-1 CH14
hide	< AW V 1 3	AD16DA-1.AO 02.CURVE 2D	hide	< AW_V_1_15	AD16DA-1.AO_08.CURVE_2D	hide	< AW_V_1_27	AD16DA-1.AO_14.CURVE_2D
hide	< AW_M_1_3	(1.0)	hide	< AW_M_1_15	(1.0)	hide	< AW_M_1_27	(1.0)
hide	< AW_C_1_4		hide	< AW_C_1_16		hide	< AW_C_1_28	
hide	< AW_V_1_4		hide	< AW_V_1_16		hide	< AW_V_1_28	
hide	< AW M 1 4	(1.0)	hide	< AW_M_1_16	(1.0)	hide	< AW_M_1_28	(1.0)
hide	< AW_C_1_5	16DA-1 CH3	hide	< AW_C_1_17	16DA-1 CH9	hide	< AW_C_1_29	16DA-1 CH15
hide	< AW V 1 5	AD16DA-1.AO_03.CURVE_2D	hide	< AW_V_1_17	AD16DA-1.AO_09.CURVE_2D	hide	< AW_V_1_29	AD16DA-1.AO_15.CURVE_2D
hide	< AW_M_1_5	(1.0)	hide	< AW_M_1_17	(1.0)	hide	< AW_M_1_29	(1.0)
hide	< AW_C_1_6		hide	< AW_C_1_18		hide	< AW_C_1_30	
hide	< AW V 1 6		hide	< AW_V_1_18		hide	< AW_V_1_30	
hide	< AW_M_1_6	(1.0)	hide	< AW_M_1_18	(1.0)	hide	< AW_M_1_30	(1.0)
hide	< AW C 1 7	16DA-1 CH4	hide	< AW_C_1_19	16DA-1 CH10	hide	< AW_C_1_31	16DA-1 CH16
hide	< AW V 1 7	AD16DA-1.AO 04.CURVE 2D	hide	< AW_V_1_19	AD16DA-1.AO_10.CURVE_2D	hide	< AW_V_1_31	AD16DA-1.AO_16.CURVE_2D
hide	< AW M 1 7	[1.0]	hide	< AW_M_1_19	(1.0)	hide	< AW_M_1_31	(1.0)
hide	< AW C 1 8		hide	< AW_C_1_20		hide	< AW_C_1_32	
hide	< AW V 1 8		hide	< AW_V_1_20		hide	< AW_V_1_32	
hide	< AW M 1 8	(1.0)	hide	< AW_M_1_20	(1.0)	hide	< AW_M_1_32 👻	(1.0)
hide	< AW C 1 9	16DA-1 CH5	hide	< AW_C_1_21	16DA-1 CH11	,	,	,
hide	< AW V 1 9	AD16DA-1.AO 05.CURVE 2D	hide	< AW_V_1_21	AD16DA-1.AO_11.CURVE_2D			
hide	< AW M 1 9	[1.0]	hide	< AW_M_1_21	(1.0)			
hide	< AW_C_1_10		hide	< AW_C_1_22				
hide	< AW V 1 10		hide	< AW_V_1_22				
hide	< AW M 1 10	(1.0)	hide	< AW_M_1_22	(1.0)			
hide	< AW_C 1 11	16DA-1 CH6	hide	< AW_C_1_23	16DA-1 CH12			
hide	< AW V 1 11	AD16DA-1.AO 06.CURVE 2D	hide	< AW_V_1_23	AD16DA-1.AO_12.CURVE_2D			
hide	< AW_M_1_11	[1.0]	hide	< AW_M_1_23	(1.0)			
hide	< AW C 1 12		hide	< AW_C_1_24				
hide	< AW V 1 12		hide	< AW_V_1_24				
hide	< AW M 1 12	(1.0)	hide	< AW_M_1_24	(1.0)			

Figure 6-106. MODBUS\_M Block Analog Write RPT Example

## Automation Direct Modbus Interface (T1K-MODBUS) Module



In this example, the T1K-MODBUS adapter was set up for RS-232 communications. The T1K-MODBUS RS-232 communications setup must be configured manually with DIP switches located on the Adapter. These DIP switches must agree with the settings specified in the MOD\_PORT and MODBUS\_M blocks. The MOD\_PORT block uses 8 data bits per word. The settings for this example are shown in Figure 6-107, T1K-MODBUS Dip Switch Settings.





This configures the module for 38,400 Baud rate (Sw1-3), default communication setting mode (Sw4), hold outputs off (Sw5), 9600 bps for RJ12 connection (Sw6), 584/984 Modbus slave addressing mode (Sw7), and disable the CTS pin on the RJ12 connector (Sw8). Because the default communications mode is selected, the RJ12 connection is not used. The default communications mode is set for 8 bit communications data, 1 start bit, 1 stop bit, odd parity, 1second communication timeout, and 0 ms RTS Delay time. The MOD\_PORT GAP block settings must match these communication settings when configured.

The T1K-MODBUS adapter will support RS-232, RS-422, and RS-485 connections. In this example, the connection between the AtlasPC control communications port (Comm 02) and the T1K-MODBUS adapter was wired as a RS-232 connection. See Figure 6-108 for example of RS-232 connection.





The Automation Direct T1K-MODBUS adapter doesn't reserve any read or write addresses for status words as the Allen-Bradley unit did.

## Automation Direct Discrete Input (Sink) (T1K-08ND3) Module



The T1K-08ND3 can be configured for sink or source detection with internal or external power. In this example, the unit is configured for sink mode with external power. This configuration is set up with jumpers located on the module. See Figure 6-109 for T1K-08ND3 Sink/External Power Configuration.

Sink Module							
MODULE			1				
SOURCE	00	00000	INT				
SINK			EXT				

Figure 6-109. T1K-08ND3 Sink/External Power Configuration

See Figure 6-110 for example of T1K-08ND3 module wiring.
DIST Automation	RIBUTED I/O n Direct T1K-08ND	3
Disc		
	Input	Input 0
MBI.A1.A02.G1.N1_BI_01	Common	Com0-0
	Internal Supply Voltage	V0-0
	Input	Input 1
MBI.A1.A02.G1.N1_BI_02	Common	Com0-1
	Internal Supply Voltage	V0-1
	Input	Input 2
MBI.A1.A02.G1.N1_BI 03	Common	Com0-2
	Internal Supply Voltage	V0-2
	Input	Input 3
MBI.A1.A02.G1.N1_BI_04	Common	Com0-3
	Internal Supply Voltage	V0-3
	Input	Input 4
MBI.A1.A02.G1.N1_BI_05	Common	Com1-4
	Internal Supply Voltage	V1-4
	Input	Input 5
MBI.A1.A02.G1.N1_BI_06	Common	Com1-5
	Internal Supply Voltage	V1-5
	Input	Input 6
MBI.A1.A02.G1.N1_BI_07	Common	Com1-6
	Internal Supply Voltage	V1-6
	Input	Input 7
MBI.A1.A02.G1.N1_BI_08	Common	Com1-7
	Internal Supply Voltage	V1-7



The T1K-08ND3 memory map indicates that there is one read byte (8 bits) address and no write addresses. See Figure 6-111 for memory map of Automation Direct T1K-08ND3 Discrete input module.

Memo	Memory Map of 8-Point Discrete Input Modules (T1K–08NA–1 and T1K–08ND3)												
Decimal Bit	07	06	05	04	03	02	01	00	Sizo				
Octal Bit	Octal Bit 07 06 05 04 03 02 01 00												
	X7 X6 X5 X4 X3 X2 X1 X0 Read Byte												
	Write Byte 1												

Figure 6-111	. T1K-08ND3	Memory Map
--------------	-------------	------------

The Automation Direct T1K-08ND3 doesn't have any filter or other options to set, therefore there are no write addresses assigned. In this example, each bit is displayed using a B\_NAME block. Each block is connected to the specific address in the MODBUS\_M block RPT window shown above. See Figure 6-112 for example of T1K-08ND3 Read GAP blocks.



Figure 6-112. Example of T1K-08ND3 Read GAP Blocks

## Automation Direct Discrete Input (Sink) (T1K-16ND3) Module



The T1K-16ND3 can be configured for sink or source detection with internal or external power. In this example, the unit is configured for sink mode with external power. This configuration is set up with jumpers located on the module. See Figure 6-113 for T1K-16ND3 Sink/External Power Configuration.



Figure 6-113. T1K-16ND3 Sink/External Power Configuration

See Figure 6-114 for example of T1K-16ND3 module wiring.

DIST Automation	RIBUTED I/O n Direct T1K-16ND	3
DISC	RETE INPUT	
	Input	Input 0
MBI.A1.A02.G1.N2_BI_01	Common	Com0-0
	Internal Supply Voltage	V0-0
	Input	Input 1
MBI.A1.A02.G1.N2 BI 02	Common	Com0-1
	Internal Supply Voltage	V0-1
	Input	Input 2
MBLA1.A02.G1.N2_BL.03	Common	Com0-2
	Internal Supply Voltage	V0-2
	Incitial Supply Voltage	Input 3
	Operation	Corro 2
MBI.A1.A02.G1.N2_B1_04	Common	Como-3
	Internal Supply voltage	VU-3
	input	Input 4
MBI.A1.A02.G1.N2_BI_05	Common	Com1-4
ļ	Internal Supply Voltage	V1-4
	Input	Input 5
MBI.A1.A02.G1.N2_BI_06	Common	Com1-5
	Internal Supply Voltage	V1-5
	Input	Input 6
MBI.A1.A02.G1.N2_BI_07	Common	Com1-6
	Internal Supply Voltage	V1-6
	Input	Input 7
MBI A1 A02 G1 N2 BL 08	Common	Com1-7
	Internal Supply Voltage	V1-7
	Incitial Supply Voltage	
MPLA1 A02 C1 N2 PL 00	Common	Com2.8
MBI.A1.A02.G1.N2_D1_09	Late and Quere hub/alte as	00112-0
	Internal Supply Voltage	V2-0
	Input	Input 9
MBI.A1.A02.G1.N2_BI_10	Common	Com2-9
	Internal Supply Voltage	V2-9
1	Input	Input 10
MBI.A1.A02.G1.N2_BI_11	Common	Com2-10
	Internal Supply Voltage	V2-10
	Input	Input 11
MBI.A1.A02.G1.N2 BI 12	Common	Com2-11
	Internal Supply Voltage	V2-11
	Input	Input 12
MBLA1.A02.G1.N2_BL_13	Common	Com3-12
	Internal Supply Voltage	1/3-12
	Input	Input 13
MBL 41 402 C1 N2 BL 14	Common	Com2 12
MBI.A1.A02.G1.N2_BI_14	Common	0000-13
	Internal Supply Voltage	V3-13
	Input	Input 14
MBI.A1.A02.G1.N2_BI_15	Common	Com3-14
	Internal Supply Voltage	V3-14
	Input	Input 15
MBI.A1.A02.G1.N2_BI_16	Common	Com3-15
	Internal Supply Voltage	V3-15

Figure 6-114 Example of T1K-16ND3 Module Wiring

The T1K-16ND3 memory map indicates that there are two read byte (16 bits) addresses and no write addresses. See Figure 6-115 for memory map of Automation Direct T1K-16ND3 Discrete input module.

	Memory Map of 16-Point Discrete Input Modules (T1K–16NA–1 and T1K–16ND3)													
Decimal Bit	07	06	05	04	03	02	01	00	Sizo					
Octal Bit	Octal Bit 07 06 05 04 03 02 01 00													
	X7	X6	X5	X4	X3	X2	X1	X0	Read Byte 1					
	X17	X16	X15	X14	X13	X12	X11	X10	Read Byte 2					
	Write Byte 1													

Figure 6-115. T1K-16ND3 Memory Map

The Automation Direct T1K-16ND3 doesn't have any filter or other options to set, therefore there are no write addresses assigned. In this example, each bit is displayed using a B\_NAME block. Each block is connected to the specific address in the MODBUS\_M block RPT window shown above. See Figure 6-116 for example of T1K-16ND3 Read GAP blocks.

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Figure 6-116. Example of T1K-16ND3 Read GAP Blocks



Automation Direct Discrete Output (Sink) (T1K-16TD1) Module

In this example the T1K-16ND3 was connected to a Woodward 16 channel relay module. See Figure 6-117 for example of T1K-16ND3 module wiring.



Figure 6-117. Example of T1K-16ND3 Module to Relay Module Wiring

The T1K-16TD1 memory map indicates that there are no read byte (8 bits) addresses and two write byte (16 bits) addresses. See Figure 6-118 for memory map of Automation Direct T1K-16TD1 Discrete Output module.

ר)	Memory Map of 16-Point Discrete Input Modules (T1K–16TA, T1K–16TD1, T1K–16TD2 and T1K–16TR)												
Decimal Bit	07	06	05	04	03	02	01	00	Sizo				
Octal Bit	07	06	05	04	03	02	01	00	5126				
Not Used Read Byte 1													
	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Write Byte 1				
	Y17	Y16	Y15	Y14	Y13	Y12	Y11	Y10	Write Byte 2				

Figure 6-118. T1K-16TD1 Module Memory Map

The Automation Direct T1K-16TD1 module doesn't have any status words to read, therefore there are no read addresses assigned. In this example, each bit is written using a B\_NAME block. Each block is connected to the specific address in the MODBUS\_M block RPT window shown above. See Figure 6-119 for example of T1K-16TD1 write GAP blocks.



Figure 6-119. Example of T1K-16TD1 GAP Write Blocks

# Automation Direct Relay Output (T1K-08TRS) Module



See Figure 6-120 for example of T1K-08TRS module wiring.



Figure 6-120. Example of T1K-08TRS Module Wiring

The T1K-08TRS memory map indicates that there are no read byte addresses and one write byte (8 bits) address. See Figure 6-121 for memory map of Automation Direct T1K-08TRS Relay Output module.

Memo (1	Memory Map of 8-Point Discrete Output Modules (T1K–08TA, T1K–08TD1 and T1K–08TR)												
Decimal Bit	07	06	05	04	03	02	01	00	Sizo				
Octal Bit	Octal Bit 07 06 05 04 03 02 01 00												
	Not Used Read Byte 1												
	Write Byte 1												

Figure 6-121. T1K-08TRS Module Memory Map

The Automation Direct T1K-08TRS module doesn't have any status words to read, therefore there are no read addresses assigned. In this example, each bit is written using a B\_NAME block. Each block is connected to the specific address in the MODBUS\_M block RPT window shown above. See Figure 6-122 for example of T1K-08TRS write GAP blocks.





# Automation Direct Analog Input (T1F-16AD-1) Module



In this example, the T1F-16AD-1 is wired with loop powered transducers. See Figure 6-123 for example of T1F-16AD-1 module wiring.

DIST Automation	RIBUTED I/O Direct T1F-16AD-1	I					
ANA	LOG INPUT					$\cap$	
	Input	Input 0		[	1 -	-( -20mA Source)	-
MBI.A1.A02.G1.N5_AI_01	Common	Com0-0		_			
	External Supply Voltage	V0-0			2		+
	Input	Input 1		[	3	-{ -20mA Source/	
MBI.A1.A02.G1.N5_AI_02	Common	Com0-1				$\bigcirc$	
	External Supply Voltage	V0-1		_		2000	+
	Input	Input 2			5	Source	
MBI.A1.A02.G1.N5_AI_03	Common	Com0-2				$\bigcirc$	
	External Supply Voltage	V0-2	1	_			+
	Input	Input 3			7	-{ Source/	· ·
MBI.A1.A02.G1.N5_AI_04	Common	Com0-3				$\bigcirc$	
	External Supply Voltage	V0-3		_			+
	Input	Input 4			9	-{ -20mA Source	· ·
MBI.A1.A02.G1.N5_AI_05	Common	Com1-4				$\bigcirc$	
	External Supply Voltage	V1-4					+
	Input	Input 5		[	11 -	-{ Source}	· ·
MBI.A1.A02.G1.N5_AI_06	Common	Com1-5				$\bigcirc$	
	External Supply Voltage	V1-5		_		(	+
	Input	Input 6			13	Source/	
MBI.A1.A02.G1.N5_AI_07	Common	Com1-6				$\bigcirc$	
	External Supply Voltage	V1-6		_		2000	+
	Input	Input 7			15	Source	
MBI.A1.A02.G1.N5_AI_08	Common	Com1-7				$\bigcirc$	
	External Supply Voltage	V1-7		_		2000	+
	Input	Input 8			17	Source	
MBI.A1.A02.G1.N5_AI_09	Common	Com2-8				$\bigcirc$	
	Common Supply Voltage	V2-8		_		-20m4	+
	Input	Input 9			19	Source	
MBI.A1.A02.G1.N5_AI_10	Common	Com2-9				$\sim$	
	Common Supply Voltage	V2-9		_		-20mA	+
	Input	Input 10			21	Source	
MBI.A1.A02.G1.N5_AI_11	Common	Com2-10				$\leq$	
	Common Supply Voltage	V2-10		-		-20mA	+
	Input	Input II		L	23	Source	
MBI.A1.A02.G1.N5_AI_12	Common	Com2-11				$\leq$	
	Common Supply Voltage	V2-11		-	-	-20mA	+
	Input	Com2 12			25	Source	
WIDI.A 1.AUZ.G 1.IN5_AI_13	Common Sunniu Voltage	V2 12				$\leq$	
	Common Supply Voltage	V3-12		-	-	-20mA	+
	Input	Com2 12			2/	Source	
WBI.A1.A02.01.N0_AI_14	Common Sunniu Voltage	V2 12				$\sim$	
	Common Supply Vollage	V3-13		-		(-20mA	+
MBI &1 &02 G1 N5 AL 15	Common	Com3-14			20	Source	
MIDI.A 1.A02.0 1.N0_AI_15	Common Supply Volters	V2 14				$\sim$	
	Input	100ut 15		Г	21 -		+
MBLA1 A02 G1 N5 AL 16	Common	Com3-15				Source	
MDI.A 1.A02.01.N0_AI_10	Common Supply Voltage	V3-15			►To +24VF	ົ້ວແ	
	Common Supply Voltage	VJ-15		-	To 24CO	М	

Figure 6-123. Example of T1F-16AD-1 Module Wiring

The T1F-16AD-1 memory map indicates that there are 64 read byte (32 words) addresses and no write byte addresses. See Figure 6-124 for memory map of Automation Direct T1F-16AD-1 Analog Input module.

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Memo	ory N	lap o	of 1	6-C	har	nel	Anal	og Ir	nput	Module	Decimal Bit 07 06 05 04 03 02 01 0					00	Cine			
				(T	1F-	-16A	D)				Octal Bit	07	06	05	04	03	02	01	00	Size
Decimal Bit	07	06	0	5 (	04	03	02	01	00	Size			A	nalog	y Valu	e Ch	anne	19		Read Byte 33
Octal Bit	07	06	0	5 (	04	03	02	01	00				A	nalog	g Valu	e Ch	anne	19		Read Byte 34
		Ar	nal	og V	/alu	e Ch	anne	1		Read Byte 1		not used							Byte35	
		Ar	nal	og V	alu	e Cł	anne	1		Read Byte 2			ň	eserv	/ed fo	r futu	ire us	5e		Byte36
				n	iot i	used				Byte3			An	alog	Value	e Cha	annel	10		Read Byte 37
		re	354	rve	d for	r futi	ure u:	se		Byte4			Ar	alog	Value	e Cha	annel	10		Read Byte 38
		Ar	nal	og V	/alu	e Cł	anne	12		Read Byte 5					not u	used				Byte39
		Ar	nal	og V	/alu	e Cł	anne	12		Read Byte 6			n	eserv	/ed fo	r futu	ire us	se		Byte40
				n	iot i	used				Byte7			Ar	nalog	Value	e Cha	annel	11		Read Byte 41
		re	356	rve	d fo	r futi	ure u:	se		Byte8			Ar	alog	Value	e Cha	annel	11		Read Byte 42
		Ar	nal	og V	/alu	e Cł	anne	13		Read Byte 9					not u	used				Byte43
		Ar	nal	og V	/alu	e Cł	anne	13		Read Byte 10			n	eserv	/ed fo	r futu	ire us	5e		Byte44
				n	iot i	Jsed				Byte11			An	alog	Value	e Cha	annel	12		Read Byte 45
		re	356	rve	d fo	r futi	ure u:	se		Byte12			An	alog	Value	e Cha	annel	12		Read Byte 46
		Ar	nal	og V	/alu	e Cł	anne	4		Read Byte 13			not used					Byte47		
		Ar	nal	og V	/alu	e Cł	anne	4		Read Byte 14			reserved for future use				Byte48			
				n	ιot ι	used				Byte15			An	alog	Value	e Cha	annel	13		Read Byte 49
		re	356	rve	i fo	r futi	ure u:	se		Byte16			An	alog	Value	e Cha	annel	13		Read Byte 50
		Ar	nəl	og V	/alu	e Ch	anne	15		Read Byte 17					not u	used				Byte51
		Ar	nal	og V	/alu	e Cł	anne	15		Read Byte 18			n	eserv	/ed fo	r futu	ire us	se		Byte52
				n	ιot ι	used				Byte19			An	alog	Value	e Cha	annel	14		Read Byte 53
		re	356	rve	i fo	r futi	ure us	se		Byte20			An	alog	Value	e Cha	annel	14		Read Byte 54
		Ar	nal	og V	/alu	e Cł	anne	el 6		Read Byte 21					not u	used				Byte55
		Ar	nal	og V	/alu	e Cł	anne	el 6		Read Byte 22			n	eserv	/ed fo	r futu	ire us	se		Byte56
				n	iot i	used				Byte23			An	alog	Value	e Cha	annel	15		Read Byte 57
		re	356	rve	i fo	r futi	ure u:	se		Byte24			An	alog	Value	e Cha	annel	15		Read Byte 58
		Ar	nal	og V	/alu	e Cł	anne	17		Read Byte 25		not used					Byte59			
		Ar	nal	og V	/alu	e Cł	anne	el 7		Read Byte 26		reserved for future use					Byte60			
				n	iot i	used				Byte27		Analog Value Channel 16					Read Byte 61			
		re	356	rve	d fo	r futi	ure u:	se		Byte28			An	alog	Value	e Cha	annel	16		Read Byte 62
		Ar	nəl	og V	/alu	e Ch	anne	8 18		Read Byte 29				-	not u	used				Byte63
		Ar	nal	og V	/alu	e Ch	anne	8 18		Read Byte 30		1	n	eser	/ed fo	r futu	ire us	se		Byte64
				n	iot i	used				Byte31			N	ot Us	ed					Write Byte 1
		re	204	erve	i fo	r futi	ire us	se		Byte32										

Figure 6-124. T1F-16AD-1 Analog Input Module Memory Map

To scale the analog input for the T1F-16AD-1 module, CURVE 2D blocks were used. For the GAP block to convert the raw counts read from the T1F-16AD-1 module to engineering units, the relationship between raw counts and engineering units is specified in the CURVE\_2D block. The raw count to milliamp relationship can be found in the Automation Direct manual T1K-INST-M. See Figure 6-125 for Current Input Module Resolution. The charts specify counts in decimal form. In this example, the 0-20mA scaling graph was used. The CURVE 2D block can be scaled to output any engineering units desired. In this example, the CURVE 2D block was scaled to output 0-20mA when 0-20mA is seen by the module. The X\_1 field specifies the module output counts when the module input is at zero mA. The X 2 field specifies the module output counts when the input is at 20mA. The Y 1 field specifies the block output in milliamps when the input counts are 0. The  $\overline{Y}$  2 field specifies the block output in milliamps when the input is at maximum counts (8191). The CURVE 2D X 1 and Y 1 fields have been set up as tunable so that the block can be set for a 4-20mA scale if desired. See Figure 6-126 for example of T1F-16AD-1 GAP CURVE\_2D scaling blocks.



Figure 6-125. T1F-16AD-1 Current Input Module Resolution

Since each channel has two read words, each block address is incremented by two, starting at 30001 and going to 30031.





# Automation Direct Analog Output (T1F-16DA-1) Module



See Figure 6-127 for example of T1F-16DA-1 module wiring.

Automation Direct T1F-16DA-1 ANALOG OUTPUT  MBI A1 A02 G1 NE_A0_01  Output Output 0  O	DIST	RIBUTED I/O				
ANALOG OUTPUT         MBIA1.A02.G1 N6_A0_02         Common         Common <th>Automation</th> <th>Direct T1F-16DA-</th> <th>1</th> <th></th> <th></th> <th></th>	Automation	Direct T1F-16DA-	1			
ANALOG OUTPUT           MBIA1A02.G1N6_A0_01         Output         Output 0         Output 0         Output 0           MBIA1A02.G1N6_A0_02         Common         Com0-0         2			-			
Output         Output         Output         Output           MBI A1.402.G1 NB_AO_01         Common         Common         Common         Common           MBI A1.402.G1 NB_AO_02         Common         Common         Common         Common         Common           MBI A1.402.G1 NB_AO_02         Common         Common <t< th=""><th>ANAI</th><th>LOG OUTPUT</th><th></th><th></th><th></th><th><math>\frown</math></th></t<>	ANAI	LOG OUTPUT				$\frown$
MBI A1 A02. G1 NE, AO, D1         Common         Com0-0           MBI A1 A02. G1 NE, AO, D2         Common         Com0-1           External Supply Voltage         VO-0         2           MBI A1 A02. G1 NE, AO, D2         Common         Com0-1           Output         Output         Output         S           MBI A1 A02. G1 NE, AO, D3         Common         Com0-2           Output         Output         Output         S           MBI A1 A02. G1 NE, AO, D4         Common         Common         Com0-3           Output         Output         Output         Output         S           MBI A1 A02. G1 NE, AO, D6         Common         Common         Com1-4         B         Common           MBI A1 A02. G1 NE, AO, D6         Common         Com1-5         S         S         Common           MBI A1 A02. G1 NE, AO, D6         Common         Com1-5         S </th <th></th> <th>Output</th> <th>Output 0</th> <th> </th> <th></th> <th>- (-20mA) +</th>		Output	Output 0	 		- (-20mA) +
External Supply Voltage         V0-0         2           MBI A1 A02. G1 N6_A0_02         Common         Common         Com0-1           MBI A1 A02. G1 N6_A0_02         Common         Com0-1         S         Common           MBI A1 A02. G1 N6_A0_02         Common         Com0-2         S         Common         Com0-3           MBI A1 A02. G1 N6_A0_04         Common         Common         Com0-3         S         Common         Com0-4           MBI A1 A02. G1 N6_A0_05         Common         Common         Com1-4         P         Common         Com0-7           MBI A1 A02. G1 N6_A0_06         Common         Com1-4         P         Common         Com0-7           MBI A1 A02. G1 N6_A0_06         Common         Com1-4         P         Common         Com0-7           MBI A1 A02. G1 N6_A0_06         Common         Com1-6         T         Common         Com0-7           MBI A1 A02. G1 N6_A0_06         Common         Com1-6         T         Common         Com0+ +           MBI A1 A02. G1 N6_A0_06         Common         Com7-7         Com0+ +         Com0+ +         Com0+ +           MBI A1 A02. G1 N6_A0_06         Common         Com7-7         Com0+ +         Com+ +         Com+ +           M	MBI.A1.A02.G1.N6_AO_01	Common	Com0-0			
Output         Output         Output           MBI A1 A02. G1 N6_AO_02         Common		External Supply Voltage	V0-0			
MBIA1.402.G1 N6_A0_02       Common       Com0-1         ABIA1.402.G1 N6_A0_02       Common       Com0-2         MBIA1.402.G1 N6_A0_04       Output       Output         Common       Com0-3       Com0-4         MBIA1.402.G1 N6_A0_04       Output       Output         Common       Com0-3       Com0-4         MBIA1.402.G1 N6_A0_04       Output       Output         Common       Com1-4       Com0-7         MBIA1.402.G1 N6_A0_06       Common       Common         Common       Com1-4       Common         MBIA1.402.G1 N6_A0_06       Common       Common         Common       Com1-5       Toternal Supply Voltage       V1-4         MBIA1.402.G1 N6_A0_06       Common       Com1-5       Toternal Supply Voltage       V1-6         MBIA1.402.G1 N6_A0_08       Output       Output       Output 6       Toternal Supply Voltage       V1-6         MBIA1.402.G1 N6_A0_08       Common Com2-8       Common Com2-8       Common Supply Voltage       V2-9         Output       Output 0       Output 10       Output 10       Com2-11       Com+ +         MBIA1.402.G1 N6_A0_10       Common Supply Voltage       V2-9       Com+ +       Com+ +         MBIA1.402.G1 N6_A0_11 </td <td></td> <td>Output</td> <td>Output 1</td> <td></td> <td>- 3</td> <td>- ( -20mA) +</td>		Output	Output 1		- 3	- ( -20mA) +
External Supply Voltage         V0-1           MBI A1 A02.G1 N6_A0_03         Common         Com0-2           External Supply Voltage         V0-3         7         Com0+           MBI A1 A02.G1 N6_A0_04         Common         Com0-3         7         Com++           MBI A1 A02.G1 N6_A0_04         Common         Com0-3         7         Com++           MBI A1 A02.G1 N6_A0_04         Common         Com0-3         7         Com++           MBI A1 A02.G1 N6_A0_05         Common         Com1-4         External Supply Voltage         V1-4           MBI A1 A02.G1 N6_A0_06         Common         Com1-6         11         Com++           MBI A1 A02.G1 N6_A0_07         Common         Com1-7         External Supply Voltage         V1-5           MBI A1 A02.G1 N6_A0_08         Common         Com1-7         External Supply Voltage         V1-7         Com++           MBI A1 A02.G1 N6_A0_08         Common         Com1-7         External Supply Voltage         V1-7         Com++           MBI A1 A02.G1 N6_A0_08         Common         Com1-7         External Supply Voltage         V2-8         Common         Com++           MBI A1 A02.G1 N6_A0_09         Common         Com2-9         Common         Com++         Com++	MBI.A1.A02.G1.N6_AO_02	Common	Com0-1			
Output         Output         Output           MBI A1.A02.G1.N6_A0.03         Common         Common         Common         Common           MBI A1.A02.G1.N6_A0.04         Output         Output <td></td> <td>External Supply Voltage</td> <td>V0-1</td> <td></td> <td></td> <td><math>\frown</math></td>		External Supply Voltage	V0-1			$\frown$
MBIA1.402.G1.N6_A0_03       Common       Com0-2         External Supply Voltage       V0-2         MBIA1.402.G1.N6_A0_04       Common       Com0-3         MBIA1.402.G1.N6_A0_05       Output       Output         Output       Output 4       0         MBIA1.402.G1.N6_A0_05       Common       Com1-3         External Supply Voltage       V1-4       0         MBIA1.402.G1.N6_A0_05       Common       Com1-5         Common       Com1-6       11       - 20m) +         MBIA1.A02.G1.N6_A0_06       Common       Com1-6         Common       Com1-7       -       20m) +         MBIA1.A02.G1.N6_A0_07       Common       Com1-6         External Supply Voltage       V1-4       -       -         MBIA1.A02.G1.N6_A0_08       Common       Com1-7       -       -         MBIA1.402.G1.N6_A0_08       Common Supply Voltage       V1-7       -       -       -         MBIA1.402.G1.N6_A0_11       Common Supply Voltage       V2-8       -       -       -       -         MBIA1.402.G1.N6_A0_11       Common Supply Voltage       V2-9       -       -       -       -       -       -       -       -       -       - <t< td=""><td></td><td>Output</td><td>Output 2</td><td></td><td>5</td><td>- ( -20mA) +</td></t<>		Output	Output 2		5	- ( -20mA) +
External Supply Voltage         V0-2           MBIA1.A02.G1 N6_A0_04         Output         Output3           MBIA1.A02.G1 N6_A0_05         Common         Com0-3           MBIA1.A02.G1 N6_A0_05         Common         Com1-3           MBIA1.A02.G1 N6_A0_05         Common         Com1-4           MBIA1.A02.G1 N6_A0_05         Common         Com1-4           MBIA1.A02.G1 N6_A0_05         Common         Com1-5           MBIA1.A02.G1 N6_A0_07         Common         Com1-5           MBIA1.A02.G1 N6_A0_07         Output         Output 0           Output         Output 6         III         -           MBIA1.A02.G1 N6_A0_07         Common Com1-7         III         -           MBIA1.A02.G1 N6_A0_08         Common Com1-7         III         -           MBIA1.A02.G1 N6_A0_09         Common Com1-7         IIII         -           MBIA1.A02.G1 N6_A0_09         Common Com2-8         III         -           Common Supply Voltage         V2-9         -         -         -           MBIA1.A02.G1 N6_A0_12         Common Com2-10         -         -         -           MBIA1.A02.G1 N6_A0_12         Common Supply Voltage         V2-10         -         -         -           MBI	MBI.A1.A02.G1.N6_AO_03	Common	Com0-2			
Output         Output 3         T         Common           MBIA1.A02.G1.N6_A0_04         Common         ComO-3         ComO-3         ComO-3           MBIA1.A02.G1.N6_A0_05         Output         Output         Output 4         0         ComO-3           MBIA1.A02.G1.N6_A0_05         Common         ComT-4         9         -         ComA) +           MBIA1.A02.G1.N6_A0_05         Common         ComT-5         External Supply Voltage         V1-4         0           MBIA1.A02.G1.N6_A0_06         Common         Common         Com1-5         External Supply Voltage         V1-6         11         -         ComA) +           MBIA1.A02.G1.N6_A0_07         Common         Common         Com1-6         External Supply Voltage         V1-7         Common         ComA) +         ComM +         C		External Supply Voltage	V0-2			$\frown$
MBIA1.02.G1.N6_A0.04       Common       Com/o         MBIA1.02.G1.N6_A0.04       Common       Common       Com/o         MBIA1.02.G1.N6_A0.05       Common       Com/o       Com/o         MBIA1.02.G1.N6_A0.06       Common       Com/o       Com/o         MBIA1.02.G1.N6_A0.06       Common       Com/o       Com/o         MBIA1.02.G1.N6_A0.06       Common       Com/o       Com/o         MBIA1.02.G1.N6_A0.07       Common       Com/o       Com/o         MBIA1.02.G1.N6_A0.08       Common       Com/o       Com/o         MBIA1.02.G1.N6_A0.08       Common Com1-6       To       Com/o         MBIA1.02.G1.N6_A0.08       Common Com1-7       External Supply Voltage       V1-5         MBIA1.02.G1.N6_A0.08       Common Com1-7       External Supply Voltage       V1-7         MBIA1.02.G1.N6_A0.09       Common Com2-78       To       Com/o         MBIA1.02.G1.N6_A0.01       Common Com2-10       Common Com2-10       Com/o         MBIA1.02.G1.N6_A0.01       Common Com2-10       Common Com2-11       Com/o         Common Supply Voltage       V2-9       Common Com2-11       Com/o       Com/o         MBIA1.02.G1.N6_A0.12       Common Com2-11       Com/o       Com/o       Com/o       C		Output	Output 3			- (-20mA +
External Supply Voltage         V0-3           MBI A1.A02.G1 N6_A0_05         Output         Output         Output 4           MBI A1.A02.G1 N6_A0_05         Common         Com1-4           External Supply Voltage         V1-4         1         -           MBI A1.A02.G1 N6_A0_05         Common         Com1-7         -         Common           MBI A1.A02.G1 N6_A0_05         Common         Com1-7         -         Common         -           MBI A1.A02.G1 N6_A0_07         Common         Com1-7         -         Common         -         Comy +           MBI A1.A02.G1 N6_A0_08         Output         Output         Output 7         -         Comy +           MBI A1.A02.G1 N6_A0_08         Common Com1-7         -         -         Comy +           MBI A1.A02.G1 N6_A0_08         Common Com2-8         -         -         Comy +           MBI A1.A02.G1 N6_A0_10         Common Supply Voltage         V2-9         -         Comy +           MBI A1.A02.G1 N6_A0_11         Common Supply Voltage         V2-9         -         Comy +           MBI A1.A02.G1 N6_A0_12         Common Supply Voltage         V2-10         -         Comy +           MBI A1.A02.G1 N6_A0_12         Common Supply Voltage         V2-10         <	MBI.A1.A02.G1.N6_AO_04	Common	Com0-3			Load
Output         Output 4         9         0         <		External Supply Voltage	V0-3			
MBIA1.402.G1.N6_A0.05       Common       Com1.4         MBIA1.402.G1.N6_A0.05       Common       Com1.4         MBIA1.402.G1.N6_A0.05       Common       Com1.5         MBIA1.402.G1.N6_A0.07       Output S       11         MBIA1.402.G1.N6_A0.07       Output S       13         MBIA1.402.G1.N6_A0.08       Output S       13         MBIA1.402.G1.N6_A0.09       Common       Com1.7         External Supply Voltage       V1.6         MBIA1.402.G1.N6_A0.08       Common       Com1.7         External Supply Voltage       V1.7         Output       Output 8       17         MBIA1.402.G1.N6_A0.08       Common Com1.7         Common Supply Voltage       V2.8         Common Supply Voltage       V2.9         MBIA1.402.G1.N6_A0.11       Common Com2.9         Common Supply Voltage       V2.10         MBIA1.402.G1.N6_A0.11       Common Supply Voltage         Output       Output 10       Com2.11         Common Supply Voltage       V2.10         MBIA1.402.G1.N6_A0.14       Output 0         MBIA1.402.G1.N6_A0.14       Output 0         Output       Output 10       Com2.11         Common Supply Voltage       V3.12 <t< td=""><td></td><td>Output</td><td>Output 4</td><td></td><td></td><td>- (-20mA) +</td></t<>		Output	Output 4			- (-20mA) +
External Supply Voltage         V1-4           Output         Outputs           Output         Outputs           Output         Outputs           MBI A1 A02.G1 N6_A0_06         Common           Common         Com1-5           External Supply Voltage         V1-5           MBI A1 A02.G1 N6_A0_07         Common           MBI A1 A02.G1 N6_A0_08         Common           Common         Com1-7           External Supply Voltage         V1-8           MBI A1 A02.G1 N6_A0_08         Common           Common Supply Voltage         V2-8           Output         Output 9           MBI A1 A02.G1 N6_A0_08         Common Com2-8           Common Supply Voltage         V2-8           Output         Output 1           Output         Outpu	MBI.A1.A02.G1.N6_AO 05	Common	Com1-4			Load
Output         Output 5         TT         Common         Comm1-5           MBIA1A02.G1.N6_A0.06         Common         Comm1-5         TT         Common           MBIA1.A02.G1.N6_A0.07         Output 7         Output 6         TT         Common           MBIA1.A02.G1.N6_A0.07         Common         Com1-6         TT         Common           MBIA1.A02.G1.N6_A0.08         Common         Com1-7         TT         Common           MBIA1.A02.G1.N6_A0.08         Common         Com1-7         TT         Common           MBIA1.A02.G1.N6_A0.09         Common         Common Supply Voltage         V1-7         TT         Common           MBIA1.A02.G1.N6_A0.09         Common Supply Voltage         V1-7         TT         Common         Com1-7           MBIA1.A02.G1.N6_A0.09         Common Supply Voltage         V2-8         TT         Common         Com1+7           MBIA1.A02.G1.N6_A0.12         Common Supply Voltage         V2-9         TT         Common         Com1+7           MBIA1.A02.G1.N6_A0.12         Common Supply Voltage         V2-10         Common         Com1+7         Common         Com1+7           MBIA1.A02.G1.N6_A0.12         Common Supply Voltage         V2-10         Com1+1         Com1+1         Com1+1		External Supply Voltage	V1-4			-
MBIA1.402.G1.N6_A0_06         Common         Com1-5           External Supply Voltage         V1-5           MBIA1.402.G1.N6_A0_07         Common           Common         Com1-5           MBIA1.402.G1.N6_A0_07         Common           MBIA1.402.G1.N6_A0_07         Common           MBIA1.402.G1.N6_A0_08         Common           Common         Com1-7           External Supply Voltage         V1-7           Output         Output 7           Output         Output 8           Common Supply Voltage         V2-8           Output         Output 10           Output         Output 11           Common Supply Voltage         V2-10           Output         Output 11           Common Supply Voltage         V2-11           Output         Output 11           Common Supply Voltage         V2-11           Output         Output 11           MBIA1.402.G1.N6_A0_14         Common Com3-12 <td></td> <td>Output</td> <td>Output 5</td> <td></td> <td></td> <td>- (-20mA +</td>		Output	Output 5			- (-20mA +
External Supply Voltage         V1-5           Output         Output 6           Output         Output 7           MBI A1 A02.G1 N6_AO, 07         Common           Common Com1-6         External Supply Voltage         V1-6           Output         Output 7         -           MBI A1 A02.G1 N6_AO, 08         Common Com1-7         External Supply Voltage         V1-7           MBI A1 A02.G1 N6_AO, 09         Common Supply Voltage         V1-7         -           MBI A1 A02.G1 N6_AO, 09         Common Supply Voltage         V2-8         -         -           Output         Output         Output 9         15         -         -           MBI A1 A02.G1 N6_AO, 01         Common Supply Voltage         V2-9         -         -         -           MBI A1 A02.G1 N6_AO, 11         Common Supply Voltage         V2-9         -         -         -           MBI A1 A02.G1 N6_AO, 11         Common Com2-10         Common Supply Voltage         V2-10         -         -         -           MBI A1 A02.G1 N6_AO, 11         Common Com2-11         Common Com2-11         -         -         -         -         -         -         -         -         -         -         -         -         -	MBI.A1.A02.G1.N6 AO 06	Common	Com1-5			Load
Output         Output 6         13         -         Common           MBIA1.A02.G1.N6_AO_07         Common         Com1-6         -         Common         +           MBIA1.A02.G1.N6_AO_08         Common         Com1-7         -         Common         +           MBIA1.A02.G1.N6_AO_08         Common         Com1-7         -         -         Common         +           MBIA1.A02.G1.N6_AO_08         Common         Com1-7         -		External Supply Voltage	V1-5			Ä
MBIA1.402.G1N6_A0_07       Common       Common <td< td=""><td></td><td>Output</td><td>Output 6</td><td></td><td>12</td><td>- (-20mA +</td></td<>		Output	Output 6		12	- (-20mA +
External Supply Voltage         V1-6 Output         Output           MBI.A1.A02.G1.N6_A0_08         Common         Common         Com1-7 External Supply Voltage         V1-7           MBI.A1.A02.G1.N6_A0_09         Common         Common         Com2-8 Common Supply Voltage         V2-8           MBI.A1.A02.G1.N6_A0_09         Common Supply Voltage         V2-8         17         - 20m) +           MBI.A1.A02.G1.N6_A0_01         Common Supply Voltage         V2-9         - 20m) +         - 20m) +           MBI.A1.A02.G1.N6_A0_11         Common Supply Voltage         V2-9         - 20m) +         - 20m) +           MBI.A1.A02.G1.N6_A0_12         Common Supply Voltage         V2-10         - 20m) +         - 20m) +           MBI.A1.A02.G1.N6_A0_12         Common Supply Voltage         V2-10         - 20m) +         - 20m) +           MBI.A1.A02.G1.N6_A0_12         Common Supply Voltage         V2-10         - 20m) +         - 20m) +           MBI.A1.A02.G1.N6_A0_13         Common Com2-11         Common Supply Voltage         - 20m) +         - 20m) +           MBI.A1.A02.G1.N6_A0_14         Common Com3-12         Common Supply Voltage         - 20m) +         - 20m) +           MBI.A1.A02.G1.N6_A0_14         Common Com3-13         Common Supply Voltage         - 20m) +         - 20m) +	MBLA1 A02 G1 N6 AO 07	Common	Com1-6		13	Load
Dutput         Output         Output 7           MBIA1A02.G1N6_A0_0         Common         Common         Common           MBIA1.A02.G1N6_A0_09         Common         Common         Common           Common         Common         Common         Common           Common         Common         Common         Common           Common         Common         Common         Common           Common         Common         Com2-9         Common           Output         Output 11         Output 11         Common           MBIA1.A02.G1N6_A0_10         Common Com2-10         Common + Loan           Ommon         Com2-10         Common + Loan         Common           Output         Output 11         Common + Loan         Common           MBIA1.A02.G1N6_A0_12         Common Supply Voltage         V2-11         Common + Loan           MBIA1.A02.G1N6_A0_12         Common Supply Voltage         V2-11         Common + Loan         Common + Loan           MBIA1.A02.G1N6_A0_14         Common Com3-12         Common Supply Voltage         V3-12         Common + Loan         Common + Loan           MBIA1.A02.G1N6_A0_14         Common Com3-13         Common Supply Voltage         V3-14         Common + Loan         Common + Loan	100000000000000000000000000000000000000	External Supply Voltage	V1-6			$\sim$
MBIA1.A02.G1N6_A0_08       Common       Com177         External Supply Voltage       V1-7         External Supply Voltage       V1-7         MBIA1.A02.G1N6_A0_09       Common Supply Voltage       V2-8         Common Supply Voltage       V2-9         MBIA1.A02.G1N6_A0_11       Common Supply Voltage       V2-10         Output       Output 10       Output 10         Common Supply Voltage       V2-10       Common 4000000000000000000000000000000000000		Output	Output 7		15	- (-20mA +
MBLA1.A02.G1.N6_A0_13         Output	MBLA1 A02 G1 N6 AO 08	Common	Com1-7		13	Load
Dutput         Output &         Output 8           Output         Output 8         T         -         Common +           MBIA1.402.G1.N6_A0_10         Common Supply Voltage         V2-8         T         -         Common +         Common Supply Voltage         V2-8           MBIA1.402.G1.N6_A0_11         Common Common Comm2-10         Common Com2-10         T         -         Common +         Co		External Supply Voltage	V1-7			
MBIA1.A02.G1N6_A0_96       Common Common Supply Voltage       V2-8 V2-8         MBIA1.A02.G1N6_A0_10       Output Common Supply Voltage       V2-8 V2-9         MBIA1.A02.G1N6_A0_11       Common Supply Voltage       V2-9 V2-10         MBIA1.A02.G1N6_A0_11       Common Supply Voltage       V2-10 V2-10         MBIA1.A02.G1N6_A0_12       Common Supply Voltage       V2-10 V2-10         MBIA1.A02.G1N6_A0_12       Common Supply Voltage       V2-11 V2-10         MBIA1.A02.G1N6_A0_12       Common Supply Voltage       V2-11 V2-10         MBIA1.A02.G1N6_A0_12       Common Com3-12 Common Supply Voltage       V2-11 V2-11         MBIA1.A02.G1N6_A0_14       Output Output       Output 112 V1-10       27         MBIA1.A02.G1N6_A0_14       Common Com3-12 Common Supply Voltage       V3-13 V3-13         MBIA1.A02.G1N6_A0_14       Common Com3-12 Common Supply Voltage       V3-13 V3-14         MBIA1.A02.G1N6_A0_16       Common Com3-13 Common Com3-14 Common Com3-15       Common + Com3-16 V1-10         MBIA1.A02.G1N6_A0_16       Output Output 14 Common Supply Voltage       V3-14 V3-14         MBIA1.A02.G1N6_A0_16       Common Com3-16 Common Supply Voltage       V3-14 V3-14         MBIA1.A02.G1N6_A0_16       Common Com3-16 Common Supply Voltage       V3-14 V3-14		Output	Output 8		47	- (-20mA +
MBIA1A02.G1N6_AO_110         Common Supply Voltage         V2-8           MBIA1.A02.G1N6_AO_110         Common Com2-9         -         Common + Load           MBIA1.A02.G1N6_AO_110         Common Com2-9         -         Common + Load           MBIA1.A02.G1N6_AO_110         Common Com2-9         -         Common + Load           MBIA1.A02.G1N6_AO_112         Common Com2-9         -         Common + Load           MBIA1.A02.G1N6_AO_12         Common Com2-10         -         Common + Load           MBIA1.A02.G1N6_AO_12         Common Com2-11         -         -         Common + Load           MBIA1.A02.G1N6_AO_12         Common Supply Voltage         VZ-11         -         -         -           MBIA1.A02.G1N6_AO_13         Common Supply Voltage         VZ-11         -         -         -           MBIA1.A02.G1N6_AO_14         Common Com3-12         Common Supply Voltage         V3-12         -         -         -           MBIA1.A02.G1N6_AO_14         Common Com3-13         Common Supply Voltage         V3-13         -         -         -         -           MBIA1.A02.G1N6_AO_16         Common Com3-16         Common Supply Voltage         V3-14         -         -         -         -         -         -         -	MBI A1 A02 G1 N6 AO 09	Common	Com2-8			Load
Output         Output<	100000000000000000000000000000000000000	Common Supply Voltage	V2-8			
MBIA1.A02.G1.N6_A0_10         Common Common Supply Voltage         V2-9 Common Supply Voltage         10           MBIA1.A02.G1.N6_A0_11         Common Supply Voltage         V2-10 Common Supply Voltage         20           MBIA1.A02.G1.N6_A0_12         Common Supply Voltage         V2-10 Common Supply Voltage         20           MBIA1.A02.G1.N6_A0_12         Common Supply Voltage         V2-10 Common Supply Voltage         20           MBIA1.A02.G1.N6_A0_13         Common Supply Voltage         V2-11 Common Supply Voltage         20           MBIA1.A02.G1.N6_A0_13         Common Supply Voltage         V2-11 Common Supply Voltage         20           MBIA1.A02.G1.N6_A0_14         Common Supply Voltage         V3-12 Common Supply Voltage         27         Common + Common Supply Voltage           MBIA1.A02.G1.N6_A0_16         Common Supply Voltage         V3-13 Common Supply Voltage         27         Common + Common + Common Supply Voltage         29           MBIA1.A02.G1.N6_A0_16         Common Com3-114 Common Supply Voltage         V3-13         29         - Common + Com3-15         Common + Com3-15		Output	Output 9		10	- (-20mA +
MBIA1A02.G1.N6_A0_11         Common Supply Voltage         V2-9           MBIA1.A02.G1.N6_A0_14         Common Supply Voltage         V2-10           MBIA1.A02.G1.N6_A0_15         Common Com2-10         21           MBIA1.A02.G1.N6_A0_16         Common Com2-10         23           MBIA1.A02.G1.N6_A0_12         Common Com2-11         23           MBIA1.A02.G1.N6_A0_13         Common Com3-12         25           MBIA1.A02.G1.N6_A0_14         Common Supply Voltage         V2-11           MBIA1.A02.G1.N6_A0_15         Common Supply Voltage         V3-13           MBIA1.A02.G1.N6_A0_14         Common Supply Voltage         V3-14           MBIA1.A02.G1.N6_A0_15         Common Supply Voltage         V3-14           MBIA1.A02.G1.N6_A0_16         Common Com3-16         Common Supply Voltage	MBI A1 A02 G1 N6 AO 10	Common	Com2-9		19	Load
Output         Output 10         21         20000 +           MBIA1A02.G1N6_A0_11         Common Supply Voltage         V2-10         20000 +           Output         Output 10         Output 10         21         20000 +           MBIA1A02.G1N6_A0_12         Output 10         Output 11         23         -         20000 +           MBIA1A02.G1N6_A0_12         Common Supply Voltage         V2-11         20         -         20000 +           MBIA1A02.G1N6_A0_13         Common Comm3-12         Common Supply Voltage         V3-12         25         -         20000 +           MBIA1.A02.G1N6_A0_14         Common Com3-13         Common Supply Voltage         V3-13         27         -         20000 +           MBIA1.A02.G1N6_A0_14         Common Supply Voltage         V3-13         27         -         20000 +           MBIA1.A02.G1N6_A0_15         Common Supply Voltage         V3-13         20         -         20000 +           MBIA1.A02.G1N6_A0_16         Common Com3-134         Common Supply Voltage         V3-14         20         -         20000 +           MBIA1.A02.G1N6_A0_16         Common Com3-154         Common Supply Voltage         V3-14         20         -         20000 +         20000 +         20000 +         20000 +<	MDI.AT.A02.01.10_A0_10	Common Supply Voltage	V/2-9			
MBIA1.A02.G1.N6_A0_11         Common Com2-10 Common Supply Voltage         V2-10 V2-10           MBIA1.A02.G1.N6_A0_12         Common Supply Voltage         V2-10 Common Supply Voltage         V2-10 V2-11           MBIA1.A02.G1.N6_A0_13         Common Supply Voltage         V2-11 Common Supply Voltage         Com3-12 V3-12           MBIA1.A02.G1.N6_A0_13         Common Supply Voltage         V3-12 V3-12         Common Supply Voltage         V3-12 Common Supply Voltage           MBIA1.A02.G1.N6_A0_14         Common Supply Voltage         V3-12 V3-12         Common Supply Voltage         V3-12 Common Supply Voltage         Com3-16 Common Supply Voltage         Com3-16 Common Supply Voltage         Common Supply Voltage         V3-14 Common Supply Voltage         Common Supply Voltage </td <td></td> <td>Output</td> <td>Output 10</td> <td></td> <td></td> <td>- (-20mA) +</td>		Output	Output 10			- (-20mA) +
MBIA1.A02.G1.N6_AO_14         Common Supply Voltage         V/2-10           MBIA1.A02.G1.N6_AO_14         Common Supply Voltage         V/2-11           Common Supply Voltage         V/2-11         Common Supply Voltage           MBIA1.A02.G1.N6_AO_13         Common Comm2-11         Common Supply Voltage           MBIA1.A02.G1.N6_AO_14         Common Supply Voltage         V/3-12           MBIA1.A02.G1.N6_AO_15         Common Supply Voltage         V/3-13           MBIA1.A02.G1.N6_AO_16         Common Supply Voltage         V/3-13           MBIA1.A02.G1.N6_AO_16         Common Supply Voltage         V/3-14           MBIA1.A02.G1.N6_AO_16         Common Supply Voltage         V/3-14           Common Supply Voltage         V/3-14         Common Supply Voltage           MBIA1.A02.G1.N6_AO_16         Common Supply Voltage         V/3-14           Common Supply Voltage         V/3-14         Common Supply Voltage           MBIA1.A02.G1.N6_AO_16         Common Supply Voltage         V/3-14           MBIA1.A02.G1.N6_AO_16         Common Supply Voltage         V/3-14           Common Supply Voltage         V/3-15         Common Supply Voltage	MBI A1 A02 G1 N6 AO 11	Common	Com2-10			Load
Output         Output<	100000000000000000000000000000000000000	Common Supply Voltage	V/2-10			
MBIA1.A02.G1.N6_A0_12         Common Supply Voltage         V22-11           Output         Output         Output         0           MBIA1.A02.G1.N6_A0_13         Common Supply Voltage         V23-11         25         - 20mA) +           MBIA1.A02.G1.N6_A0_13         Common Supply Voltage         V3-12         - 20mA) +         1000000000000000000000000000000000000		Output	Output 11		00	- (-20mA +
MBIA1.A02.G1.N6_AO_14         Common Supply Voltage         VZ-11           MBIA1.A02.G1.N6_AO_13         Common Common Common         Common Common           MBIA1.A02.G1.N6_AO_14         Output 10         Output 13           Common Supply Voltage         V3-12         Output 13           MBIA1.A02.G1.N6_AO_14         Output 10         Output 13           Common Supply Voltage         V3-12         Output 13           MBIA1.A02.G1.N6_AO_14         Common Common Common 14         Common 14           Common Supply Voltage         V3-13         Output 14           Common Supply Voltage         V3-13         Output 14           MBIA1.A02.G1.N6_AO_15         Common Comm3.14         Common 14           Common Supply Voltage         V3-14         Output 14           MBIA1.A02.G1.N6_AO_16         Common Comm3.14         Common 14           Common Supply Voltage         V3-14         Output 15           MBIA1.A02.G1.N6_AO_16         Common Com3.15         To +24/UC	MBI A1 A02 G1 N6 AO 12	Common	Com2-11		23	Load
Output         Output 12         25         Output 12           MBIA1A02.G1N6_A0_13         Common Supply Voltage         V3-12         Output 13         27         Output 12           MBIA1A02.G1N6_A0_14         Common Supply Voltage         V3-12         Output 13         27         Output 12           MBIA1A02.G1N6_A0_14         Common Supply Voltage         V3-13         Output 13         27         Output 14           MBIA1A02.G1N6_A0_15         Common Supply Voltage         V3-13         Output 14         29         - Output 14           MBIA1.A02.G1N6_A0_15         Common Supply Voltage         V3-14         Output 14         29         - Output 14           MBIA1.A02.G1N6_A0_16         Common Com3-115         Common Supply Voltage         V3-14         0utput 15         0utput 15           MBIA1.A02.G1N6_A0_16         Common Supply Voltage         V3-15         To +24/UC         To +24/UC	MDIA1.A02.01.N0_A0_12	Common Supply Voltage	V/2-11			
MBIA1A02.G1.N6_A0_13         Common Supply Voltage         V3-12           MBIA1.A02.G1.N6_A0_14         Common Supply Voltage         V3-12           MBIA1.A02.G1.N6_A0_14         Common Supply Voltage         V3-13           MBIA1.A02.G1.N6_A0_14         Common Supply Voltage         V3-13           Common Supply Voltage         V3-13         Common Supply Voltage         V3-14           MBIA1.A02.G1.N6_A0_16         Common Com3-14         Common Supply Voltage         V3-14           MBIA1.A02.G1.N6_A0_16         Common Com3-16         Common Supply Voltage         V3-14           Common Supply Voltage         V3-14         Common Supply Voltage         V3-14           Common Supply Voltage         V3-14         Common Supply Voltage         V3-14           MBIA1.A02.G1.N6_A0_16         Common Com3-15         To +24/VDC         Common Supply Voltage		Output	Output 12			- (-20mA) +
MBIA1.A02.G1.N6_A0_16         Common Supply Voltage	MPI A1 A02 C1 N6 AO 12	Common	Com2 12		25	Load
Output         Output 13         27         -         Quint         Q	WIBI.AT.A02.01.N0_A0_13	Common Supply Voltage	V3-12			
MBI.A1.A02.G1.N6_AO_14         Common         Common Com3-13         27         Loan           MBI.A1.A02.G1.N6_AO_14         Common Supply Voltage         V3-13         -         -         20000 + +           MBI.A1.A02.G1.N6_AO_15         Common Supply Voltage         V3-14         -		Outout	Output 12			- (-20mA) +
MBLA1.A02.G1.N6_AO_16         Common Supply Voltage         V3-13           MBLA1.A02.G1.N6_AO_16         Common Common Supply Voltage         V3-14           MBLA1.A02.G1.N6_AO_16         Common Common Supply Voltage         V3-14           MBLA1.A02.G1.N6_AO_16         Common Supply Voltage         V3-14           Output 15         31         - ComA           To +24/UCC         Common Supply Voltage         V3-15	MBI A1 A02 G1 N6 AO 14	Common	Com3-12		2/	Load
Ommon Supply Voltage         VG+13         20         -         000000000000000000000000000000000000	MDIATA02.01.N0_A0_14	Common Supply Voltage	V/2 12			$\sim$
MBI.A1.A02.G1.N6_AO_15         Common		Output	Output 14			- (-20mA) +
MBLA1.A02.G1.N6_AO_16         Common Supply Voltage         V3-14	MPLA1 402 C1 N6 40 45	Common	Com2 14		29	Load
Output         Output 15           Output         Output 15           Output         Output 15           To reprint 2000 Common Com3-15         To reprint 24VDC           Common Supply Voltage         V3-14	WIDLA LAUZ.G LIND_AU_15	Common Supply Voltere	V2 14			$\leq$
MBI.A1.A02.G1.N6_AO_16         Output 15 Common Com3-15 Common Supply Voltage         V3-15		Output	0utput 45			- (-20mA) +
Milla Lauze T. No Ad _ Ito _ Common Supply Voltage V3-15	MDI 44 400 C4 NG 40 40	Common	Com2 15		31	Load
Common Supply Volage V3-13	WIDI.A1.AUZ.G1.N6_A0_16	Common Cumply Vellage	Com3-15			
		common Supply voltage	V3-15		- To 24	COM

Figure 6-127. Example of T1F-16DA-1 Module Wiring

The memory map indicates that there are no read addresses and 64 byte (32 words) write addresses. Each Analog channel uses 4 bytes. The first and second bytes of a channel contain the analog data. The third and fourth bytes are not used at this time. Channel 1 is an exception, where the 4th byte is the Module Control Byte. See Figure 6-128 for the memory map for the Automation Direct T1F-16DA-1 module.

Memo	ry Ma	ap of	16-0	ha	nnel	Anal	og O	utput	Module	Decimal Bi	07	06	05	04	4 03	02	01	00	Sizo
Desimal Di	07	0.0	(	111	-016		01	00		Octal Bit	07	06	05	04	4 03	02	01	00	0120
Decimal Bit	07	06	05	04	1 03	02	01	00	Size			Ar	halog	j Va	alue Ch	anne	el 9		Write Byte 33
Octal Bit	07	06	05	04	1 03	02	01	00	D			A	nalog	j Va	alue Ch	ann	əl 9		Write Byte 34
	_	No	t Us	ed					Read Byte 1					no	ot used				Byte35
		Ar	alog	va	lue C	nann	el 1		Write Byte 1			re	eserv	/ed	for fut	ure u	se		Byte36
		Ar	nalog	Va	lue C	hann	el 1		Write Byte 2			An	alog	Val	lue Ch	anne	10		Write Byte 37
				no	t used	1	_		Byte3			An	alog	Val	lue Ch	anne	10		Write Byte 38
		N	lodu	le (	Contr	OI By	te		Write Byte 4					no	ot used				Byte39
		Ar	halog	Va	lue C	nann	el 2		Write Byte 5			re	eserv	/ed	for fut	ure u	se		Byte40
		Ar	nalog	Va	lue C	hann	el 2		Write Byte 6			An	alog	Val	lue Ch	anne	el 11		Write Byte 41
				no	t used	1			Byte7			An	alog	Val	lue Ch	anne	el 11		Write Byte 42
		re	serv	ed	for fut	ure u	ISE		Byte8					no	ot used				Byte43
		Ar	halog	Va	lue C	hann	el 3		Write Byte 9			re	eserv	/ed	for fut	ure u	se		Byte44
		Ar	nalog	Va	lue C	hann	el 3		Write Byte 10			An	alog	Val	lue Ch	anne	12		Write Byte 45
				no	t used	1			Byte11			An	alog	Val	lue Ch	anne	12		Write Byte 46
		re	serv	ed	for fut	ure u	ISE		Byte12					no	ot used				Byte47
		Ar	nalog	Va	lue C	hann	el 4		Write Byte 13			re	eserv	/ed	for fut	ure u	se		Byte48
		Ar	nalog	Va	lue C	hann	el 4		Write Byte 14			An	alog	Val	lue Ch	anne	13		Write Byte 49
				no	t used	1			Byte15			An	alog	Val	lue Ch	anne	13		Write Byte 50
		re	serv	ed	for fut	ure u	ISB		Byte16					no	ot used				Byte51
		Ar	nalog	Va	lue C	hann	el 5		Write Byte 17			re	eserv	/ed	for fut	ure u	se		Byte52
		Ar	nalog	Va	lue C	hann	el 5		Write Byte 18			An	alog	Val	lue Ch	anne	14		Write Byte 53
				no	t used	ł			Byte19			An	alog	Val	lue Ch	anne	14		Write Byte 54
		re	serv	ed	for fut	ure u	ISƏ		Byte20					no	ot used				Byte55
		Ar	nalog	Va	lue C	hann	el 6		Write Byte 21			re	eserv	/ed	for fut	ure u	se		Byte56
		Ar	nalog	Va	lue C	hann	el 6		Write Byte 22			An	alog	Val	lue Ch	anne	15		Write Byte 57
				no	t used	1			Byte23			An	alog	Val	lue Ch	anne	15		Write Byte 58
		re	serv	ed	for fut	ure u	ISƏ		Byte24					no	ot used				Byte59
		Ar	nalog	Va	lue C	hann	el 7		Write Byte 25		reserved for future use					Byte60			
		Ar	nalog	Va	lue C	hann	el 7		Write Byte 26		Analog Value Channel 16						16 Write Byte f		
				no	t used	1			Byte27		Analog Value Channel 16						Write Byte 62		
		re	serv	ed	for fut	ure u	ISƏ		Byte28		not used					Byte63			
		Ar	nalog	Va	lue C	hann	el 8		Write Byte 29			re	eserv	/ed	for fut	ure u	se		Byte64
		Ar	nalog	Va	lue C	hann	el 8		Write Byte 30		-								
				no	t used	1			Byte31										
	reserved for future use						Byte32												

Figure 6-128. T1F-16DA-1 Module Memory Map

Since each channel has two read words, each block address is incremented by two, starting at 40001 and going to 40031. Based on the memory map and the Control Byte Table, there are 32 bits (4 bytes or 2 words) allocated for channel 1. The 4th byte (2nd word) is designated as the Module Control Byte. The control byte allows discrete bits to be set for certain functions. This byte is addressed using word address 40002. Individual bits are set using a B16\_TO\_A block to write to address 40002. See Figure 6-129 for example of the Control Byte GAP block. The first 8 bits (byte3) are not used. Bit 24 in the Control Byte Table is the IN\_9\_1 field on the block. This bit is the first bit in byte 4. In this example, Outputs Enable (bit 24) is on (True), the polarity is Unipolar (False), the Voltage Range (bit 26) is not needed and therefore set to (False), the Current Range (bit 27) is set for 0-20mA (False), and bits 28-31 are reserved and therefore set to (False). See Figure 6-130 for T1F-16DA-1 Control Byte Table.

Module Control Byte of 8&16-Channel Analog Output Module (T1F–08DA, T1F–16DA)											
Decimal Bit	31	30	29	24	Read/M/rite						
Octal Bit	37	36	35	30	iteau/write						
Bit 24		1	<b>Ou</b> 0 = A = All		Write						
Bit 25		C	<b>Unip</b> ) = U 1 = B		Write						
Bit 26			<b>5V</b> 0 1	/ <b>10\</b> = 5V = 10\	/ Rar / rang / ran	n <b>ge</b> ge ge			Write		
Bit 27		0 – 2	2 <b>0m/</b> 0 = 0 1 = 4		Write						
Bit 28 – 31	Reserved for system use								_		

Figure 6-129. T1F-16DA-1 Control Byte Table



Figure 6-130. Example of T1F-16DA-1 Control Byte GAP Block

To scale the analog output words for the T1F-16DA-1 module, CURVE 2D blocks were used. The GAP block converts the input, in milliamps, to raw counts used by the T1F-16AD-1 module. The milliamp to raw count relationship can be found in the Automation Direct manual T1K-INST-M. See Figure 6-131 for Current Output Module Resolution. The charts specify counts in decimal form. In this example, the 0-20mA scaling graph was used. The CURVE 2D block can be scaled to output any engineering units desired. In this example, the CURVE 2D block was scaled to output 0-4095 counts when 0-20mA is seen by the application. The X 1 field specifies the minimum milliamp value (0mA) from the GAP application. The X 2 field specifies the maximum milliamp value (20mA) from the GAP application. The Y\_1 field specifies the block output in counts (0 counts) when the minimum input is 0mA. The Y 2 field specifies the block output in counts (4095 counts) when the maximum input is 20mA. The CURVE 2D X 1 field has been set up as tunable so that the block can be set for a 4-20mA scale if desired. See Figure 6-132 for example of T1F-16DA-1 GAP CURVE 2D scaling blocks.







Figure 6-132. Example of T1F-16DA-1 GAP Analog Write Blocks

### Automation Direct Thermocouple Input (T1F-14THM) Module



In this example, Type K thermocouples are used. See Figure 6-133 for example of T1F-14THM module wiring.



Figure 6-133. Example of T1F-14THM Module Wiring

According to Automation Direct, the T1F-14THM module uses the same memory map as the T1F-16AD-1 module. Based on this memory map, there are 64 byte (32 words) addresses and no write byte addresses. See Figure 6-134 for memory map of Automation Direct T1F-14THM Thermocouple module.

Memory Map of 16-Channel Analog Input Module							Decimal Bit 0	it 07	06	05	(	04	)3	02	01	00	Sizo					
Dealers I Dit	0.77	0.0	0.5	(11	.F-10	5AL	J)	64	0.0		ΙΓ	Octal Bit	07	06	05	(	04	)3	02	01	00	SIZE
Decimal Bit	07	06	05	0	4 0	3	02	01	00	Size				Analog Value Channel 9			Read Byte 33					
Octal Bit	07 06 05 04 03 02 01 00							Analog Value Channel 9							Read Byte 34							
	Analog Value Channel 1				Read Byte 1				not used						Byte35							
	Analog Value Channel 1					Read Byte 2				reserved for future use						Byte36						
	not used				Byte3				Analog Value Channel 10						Read Byte 37							
	reserved for future use				Byte4				Analog Value Channel 10						Read Byte 38							
		Analog Value Channel 2				Read Byte 5				not used						Byte39						
		A	nalog	I Vê	alue (	Cha	anne	12		Read Byte 6	$  \  $			reserved for future use						Byte40		
	not used				Byte7	1 [			Analog Value Channel 11						Read Byte 41							
		ń	eserv	/ed	for fu	utur	re us	se		Byte8				Analog Value Channel 11						Read Byte 42		
		A	nalog	I Va	alue (	Cha	anne	13		Read Byte 9				not used						Byte43		
	Analog Value Channel 3			Read Byte 10				reserved for future use						Byte44								
	not used				Byte11				Analog Value Channel 12						Read Byte 45							
	reserved for future use			Byte12				Analog Value Channel 12					Read Byte 46									
	Analog Value Channel 4			Read Byte 13				not used					Byte47									
	Analog Value Channel 4				Read Byte 14				reserved for future use						Byte48							
	not used			Byte15				Analog Value Channel 13					Read Byte 49									
	reserved for future use Analog Value Channel 5			Byte16				A	halog	Vá	alue	Cha	anne	13		Read Byte 50						
				Read Byte 17				not used					Byte51									
		Analog Value Channel 5			Read Byte 18				reserved for future use						Byte52							
	not used reserved for future use			Byte19				Analog Value Channel 14						Read Byte 53								
				Byte20				A	halog	Vá	alue	Cha	anne	14		Read Byte 54						
		A	nalog	j Va	alue (	Cha	anne	16		Read Byte 21						n	iot us	ed				Byte55
	Analog Value Channel 6 not used reserved for future use Analog Value Channel 7 Analog Value Channel 7			Read Byte 22				reserved for future use Analog Value Channel 15							Byte56							
				Byte23										Read Byte 57								
				Byte24				A	alog	Va	alue	Cha	anne	15		Read Byte 58						
					Read Byte 25	]  -		+	not used						Byte59							
				Read Byte 26				reserved for future use					Byte60									
	not used reserved for future use Analog Value Channel 8				Byte27		+	Analog Value Channel 16					Read Byte 61									
					Byte28			+	Analog Value Channel 16					Read Byte 62								
					Read Byte 29	1  -		+	not used					Byte63								
	Analog Value Channel 8				Read Byte 30	-		reserved for future use						Byte64								
	not used				Byte31				Not Used						Write Byte 1							
		n	eserv	/ed	for fu	utur	re us	se		Byte32	-											

E	TAE AATLINA	The sum a second		N /	N /
Figure 6-134.	11F-141 HIVI	Inermocoup	e ivioaule	iviemorv	wap
J · · · ·					

The T1F-14THM Thermocouple module has a set of jumpers located under the top cover of the module for configuring certain parameters. See Figure 6-135 for T1F-14THM Jumper configuration Tables. In this example, the jumpers were configured for 14 channels of Type K thermocouples with output in °F and calibration disabled. See Figure 6-136 for T1F-14THM jumper locations.

## AtlasPC Digital Control, Vol. II (Distributed I/O)



Thermocouple / Voltage Inputs	Jumper							
	T/C Type 0	T/C Type 1	T/C Type 2	T/C Type 3				
J	x	x	х	х				
к		х	х	Х				
E	X		х	х				
R			х	х				
S	х	х		Х				
Т		х		Х				
В	х			х				
Ν				Х				
С	х	х	х					
0–5V.		х	х					
±5V.	х		Х					
0-156mV.			х					
±156mV.	Х	х						

#### Thermocouple Conversion Units

	Temperature Conversion Units								
Jumper	Magnitu Si °F	ide Plus gn °C	2's Complement °F °C						
Units-0	х		Х						
Units-1	Х	х							

X = Jumper Installed,

Blank Space = Jumper Removed

X = Jumper Installed, Blank Space = Jumper Remove





Figure 6-136 for T1F-14THM Jumper Locations

It has been found that the thermocouple value must be scaled to one tenth the value output by the T1K-MODBUS interface module. A divide by 10 block is used to scale the thermocouple inputs. See Figure 6-137 for example of T1F-14THM GAP DIVIDE Blocks.



Figure 6-137. Example of T1F-14THM GAP DIVIDE Blocks

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